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(71) Applicant *(for all designated States except US)*: MICRON TECHNOLOGY, INC. [US/US]; 2805 East Columbia Road, Boise, ID 83706 (US).

(72) Inventor; and
(75) Inventor/Applicant *(for US only)* : HESSON, James [US/US]; 2627 S. Swallowtail, Boise, ID 83706-6133 (US).

(74) Agent: FOX, Angus, C.; Micron Technology, Inc., 2805 East Columbia Road, Boise, ID 83706 (US).

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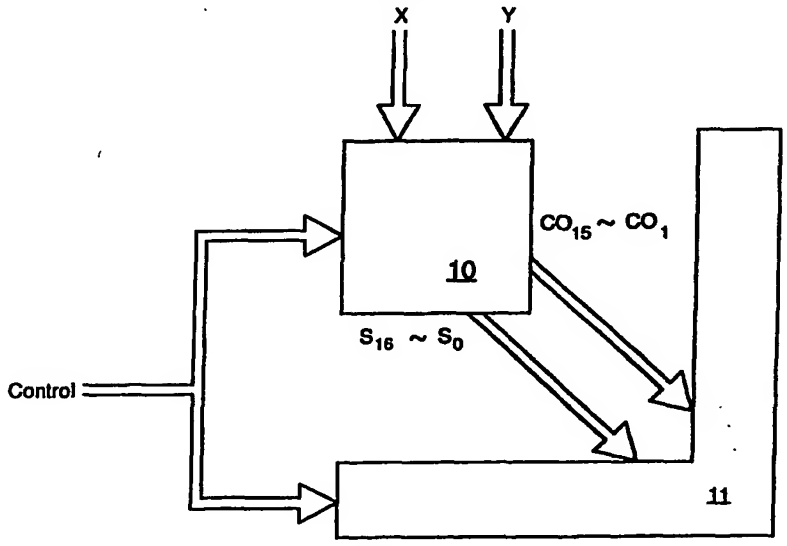

(57) Abstract

A high-speed circuit that performs unsigned mode, two's complement mode, and two types of mixed mode multiplication-accumulation with equal facility. The circuit is an array (10) constructed from ten different adder elements (FA1S, FA1A, FA2A, FAC, FACA, FACC, FAAC, FAAC3, HAC, and HAC2, which correspond to Figures 13-22, respectively). The array has two multiplier input operands (X and Y) and one accumulator term (Z), the three of which may be expressed as binary power expansions. Final addition of sumout and carryout terms of the array (10) is performed by final adder (11), which may comprise any of several possible adder configurations, including full carry lookahead, carry select, and conditional-sum type adders. Speed is accomplished through the use of high-speed adder elements having few gate delays, and by summing all even array rows together and all odd rows together, then adding the even sum with the odd sum in the final adder (11) using a Wallace tree technique. The circuit incorporates a high degree of regularity and interconnectivity, which facilitates compact circuit layout.

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UNIVERSAL MULTIPLIER-ACCUMULATOR

Field of the Invention

This invention generally relates to high-volume high-speed digital parallel processing, in particular a multiplier-accumulator integrated circuit array that will accept input operands in two's complement, unsigned magnitude, and mixed modes.

Background of the Invention

A multiplier-accumulator is a computational device that multiplies two multiplier input terms and sums the product with an accumulator term, providing a final output term. A parallel multiplier has the characteristic of operating on multiple bits within the terms simultaneously, that is, in parallel. High speed parallel multipliers and multiplier-accumulators and their efficient integration into silicon or some other semiconductor substrate have been of interest since the early days of digital computers.

Many arithmetic circuits which are widely used in the digital arts are designed for use with two's complement binary signals. While such signals and the associated circuits are particularly well adapted for performing efficiently under many circumstances, two's complement multiplication often requires the use of specialized circuits for correcting errors or characteristically incomplete results. Attempts have been made to reduce specialized circuitry in two's complement arithmetic circuits. See, for example, US patent number 3,866,030 by inventors Baugh and Wooley for a two's complement parallel array multiplier.

A multiplier-accumulator that can operate equally well acr ss two's complement, unsigned, and mixed modes is

d sirable. A first obj ctive of the present invention is, therefore, to provide a multiplier-accumulator that is universal across all modes.

Although a multiplier-accumulator has speed advantages when compared to equivalent circuits, more speed is always desirable. A second objective of the present invention is, therefore, to provide a multiplier-accumulator that has high operational speed.

It has long been recognized that an arrayed circuit structure comprised of identical or nearly-identical components facilitates circuitry layout (whether the layout is performed by hand or with computer-aided design tools). In addition, an arrayed circuit structure comprised of regular components lends itself local interconnects, which minimizes parasitic capacitance and resistance, thus increasing circuit speed. A third objective of the present invention is, therefore, to provide a universal multiplier-accumulator having an array structure with a high degree of component regularity, in order to facilitate circuit layout and minimize the length of interconnects.

Summary of the Invention

The invention is a circuit that can perform universal multiplication-accumulation. It is universal in the sense that it operates with equal facility on operands of unsigned magnitude, operands in a two's complement mode, and operands of mixed modes.

By deriving special compensation expressions for terms having negative weight for each multiplication mode (i.e., two's complement, unsigned magnitude, and mixed modes), and by grouping these compensations in a particular manner, it is possible to eliminate the need for the generation of

negative partial products. Further, by making these compensation expressions conformal across all multiplication modes, specialized circuitry is minimized and circuit regularity is maximized. Similar adder elements are arrayed, with all specialized circuitry being implemented as circuit modifications on some of these elements, thus improving circuit regularity and interconnectivity.

Fast adder elements are included to improve overall speed of the invention. Speed is further increased with the use of multiple-row addition techniques.

Brief Description of the Drawings

Figures 1a-1c depict multiplier input operands X and Y and accumulator input Z in binary form (e.g., in Figure 1a, m=8 for an 8-bit word, and each a is a bit in that word);

Figures 2a-2c depict expressions that yield magnitudes of two's complement terms X_{tc}, Y_{tc}, and Z_{tc};

Figures 2d-2f depict expressions that yield magnitudes of unsigned magnitude terms X_{uns}, Y_{uns}, and Z_{uns};

Figures 3a-3d depict expressions for the products $P_{tc}=X_{tc}\ Y_{tc}$, $P_{uns}=X_{uns}\ Y_{uns}$, $P_A=X_{tc}\ Y_{uns}$, and $P_B=X_{uns}\ Y_{tc}$, respectively;

Figures 4a-4e, 5a-5f, 6a-6f, and 7a-7e depict two-row compensation derivations for L, N, O, and Z, respectively;

Figures 8-11 depict multiplication-accumulation in unsigned mode, two's complement mode, and mixed modes A and B ("A" figures show a standard representation, "B" figures

show the representation condensed and slightly rearranged, and "C" figures show an array configuration that will perform the multiplication-accumulation);

Figure 12a is block diagram of the preferred multiplier-accumulator;

Figure 12b is a schematic of the array portion of the preferred multiplier-accumulator;

Figures 13-22 detail preferred adder elements and their operation ("A" figures are schematics of the elements, while "B" figures are logical symbols, which are used in Figure 12, for example);

Figure 23 depicts a logic diagram for a preferred Exclusive-OR (XOR) gate; and

Figure 24 depicts the logic circuitry which generates control signals TCA, TCB, TCC, and MXM.

Preferred Embodiment of the Invention

The preferred embodiment of the universal multiplier-accumulator makes use of certain algorithms, the understanding of which is essential to an understanding of the multiplier-accumulator. Therefore, a derivation of these algorithms follows.

1. Derivations

The universal multiplier-accumulator has two multiplier input operands X and Y (also called product terms) and one accumulator term Z, expressed in Figures 1a-1c as binary power expansions. The two possible accumulator input modes are two's complement and unsigned

magnitude. In this disclosure, subscript "tc" indicates two's complement mode, and subscript "uns" indicates unsigned magnitude mode. For example, X_{tc} indicates X interpreted as a two's complement number. Further, in this disclosure, a term may be represented as a vector. For example, X (shown as a binary power expansion in Figure 1) may also be represented as the vector $(a_{m-1}, a_{m-2}, \ldots, a_0)$, Y as $(b_{n-1}, b_{n-2}, \ldots, b_0)$, and Z as $(c_{m+n-1}, c_{m+n-2}, \ldots, c_0)$. Multiplication is indicated by the symbol " " and addition is indicated by the symbol "+". Logic operations are indicated in capitals, such as in the expression "a AND b", for example.

Figure 2a is a two's complement expression of X: when X is to be interpreted as X_{tc}, the expression in Figure 2a will yield the magnitude of X_{tc}. Figures 2b-2c show corresponding expressions for Y_{tc} and Z_{tc}. Figures 2d-2f show similar expressions for X_{uns}, Y_{uns}, and Z_{uns}.

Since each of the input operands X and Y can be in two's complement mode or unsigned magnitude mode, there are four possible multiplication modes for the operation P=X Y. These are two's complement mode ($P_{tc}=X_{tc}\ Y_{tc}$), unsigned magnitude mode ($P_{uns}=X_{uns}\ Y_{uns}$), mixed mode A ($P_A=X_{tc}\ Y_{uns}$), and mixed mode B ($P_B=X_{uns}\ Y_{tc}$). Figures 3a-3d, respectively, show expressions for each of these multiplication modes, based on Figures 2a-2f.

Note in Figures 3a-3d that each product includes different sign combinations of expressions L, M, N, and O. That is, $P_{tc}=+L+M-N-O$, $P_{uns}=+L+M+N+O$, $P_A=-L+M+N-O$, and $P_B=-L+M-N+O$. This is a significant observation and has bearing on the design of the preferred embodiment.

It is well known that binary addition of a two's complement form of a word is equivalent to its unsigned binary subtraction. Addition is more straightforward and

readily implemented than subtraction. To obtain a two's complement form, a word is inverted and a 1 is added to it. In the above-listed multiplication modes, terms L, N, and O are subtracted. In the preferred embodiment, "two-row compensations" are derived to aid in these subtractions. The two-row compensation L_{2RC}, for example, is a pair of rows of bits that when summed with an operand, gives a final accumulation that is as if L was subtracted. The two-row compensation contains two's complement arithmetic in a form that allows efficient design of the subject multiplier-accumulator.

Figure 4a shows the expression for term L, written the same as in Figure 3a, for example. L may also be expressed as a summation of the two rows in Figure 4b. Figure 4c shows L inverted and a 1 added to obtain a two's complement inversion, rewritten in Figure 4d. Figure 4e shows L in a two's complement binary matrix form. Figure 4e is the two-row compensation L_{2RC}.

Two-row compensation N_{2RC} is generated as shown in Figures 5a-5f. Figure 5a expresses term N, the same as in Figure 3b, for example. N may also be expressed as shown in Figure 5b. Note that b_{n-1} is a binary constant, a 1 or 0. If $b_{n-1}=1$, then N reduces to Figure 5c. If $b_{n-1}=0$, then N and its two's complement are both zero. For $b_{n-1}=1$, the two's complement of N is shown in Figure 5d. Using this information, a generalized expression for the two's complement of N can be created, shown in Figure 5e. The expression of Figure 5e is then converted to N_{2RC}, shown in Figure 5f.

Term O (Figure 6a) is similar to N. The derivation of O_{2RC}, shown in Figure 6f, is therefore derived using a similar technique.

Since the invention accumulates as well as multiplies, two-row compensation Z_{2RC} for accumulator term Z must also be derived, since Z may be positive or negative in any multiplication-accumulation mode involving two's complement. This is shown in Figures 7a-7e. Note that when $c_{m+n-1}=1$, Z<0, and when $c_{m+n-1}=0$, Z>0.

With reference to Figures 8-11, the four multiply-accumulate modes are now detailed for 8-bit X and Y terms (m=8, n=8). In each figure, a somewhat standard representation of the operation is shown, and then an equivalent, preferred arrangement. The preferred arrangements are readily adaptable to embodiment in a single circuit. M remains the same across all cases.

Figure 8a illustrates an unsigned mode multiplication-accumulation, that is, $X_{uns}\ Y_{uns}+Z_{uns}$. Elements of L, M, N and O are shown in their proper columns for addition. Figure 8b shows the same algorithm, but with O moved over the upper left edge of M. Figure 8c shows this operation in an array configuration. The correct result is obtained if addition is diagonally performed.

Figure 9a illustrates a two's complement mode multiplication-accumulation, that is, $X_{tc}\ Y_{tc}+Z_{tc}$. Recall from Figure 3a that N and O are subtracted in this mode. Instead of subtracting N and O in the preferred embodiment, two-row compensations N_{2RC} and O_{2RC} are summed. Because Z may be positive or negative in this mode, Z_{2RC} is also summed. Figure 9b shows the same derivation, but with all ones in the two-row compensations pre-summed and all but two elements of O_{2RC} moved over the upper left edge of M. For the specific case of a multiply-only algorithm (no accumulation), the inventive method reduces to the familiar Baugh-Wooley two's complement multiplier method. Figure 9c shows the operation in an array configuration. The correct result is obtained if addition is performed diagonally.

Mixed mode A (X_{tc} $Y_{uns}+Z_{tc}$) is illustrated in Figure 10a. As shown in Figure 3c, L and O are subtracted in this mode. Ther fore L_{ZRC} and O_{ZRC} are added. Z_{ZRC} is also added because Z may be positive or negative in this mode. Figure 10b shows the corresponding preferred arrangement. As in two's complement mode in Figure 9b, all ones in the two-row compensations are pre-summed. As above, Figure 10c shows an array configuration.

Finally, Figure 11a illustrates mixed mode B (X_{uns} $Y_{tc}+Z_{tc}$). As shown in Figure 3d, L and N are subtracted in this mode. Therefore L_{ZRC} and N_{ZRC} are added. Z_{ZRC} is also added because Z may be positive or negative in this mode. Figure 11c shows a corresponding array configuration.

2. Embodiment

The preferred embodiment of the invention includes an n by m multiplier array having multiple-function adder elements to perform the above-derived algorithms as represented in the array configurations of Figures 8c, 9c, 10c, and 11c. For the sake of illustration, an 8 by 8 multiplier-accumulator according to the invention is shown in Figures 12a and 12b. The preferred embodiment merges the four multiplication-accumulation modes into a single arrayed set 10 of adder elements 100-107, 110-117, 120-127, 130-137, 140-147, 150-157, 160-169, 170-179, and 180-188, detailed in Figures 13 through 23, of which the "A" figures show a schematic, and the "B" figures show a corresponding logical symbol used in Figure 12b. It is noted that some of the signals shown in the logical symbols are to interpreted differentially, and some nondifferentially. For example, SIN in Figure 14b is differential (representing true SIN and complement SIN*, shown in Figure 14a), while input a_i is not.

The elements will now b described. The following chart is provided for cross-reference:

Adder Type	Figure	Elements
FA1S	13	110, 120, 130, 140, 150, 160, 170, 172-177, 180-187
FA1A	14	111-116, 121-126, 131-136, 141-146, 151-156, 178
FA2A	15	100-106, 171
FAC	16	161-166
FACA	17	107, 117, 127, 137, 147, 157
FACC	18	167
FAAC	19	168
FAAC3	20	169
HAC	21	179
HAC2	22	188

FA1S (Figure 13) is a 3-bit fully differential full-adder cell, with propagation times of 2 gate delays from sum-in to sum-out and 1 gate delay from carry-in to carry-out, when the preferred EXOR circuit of Figure 23 is used.

FA1A (Figure 14) performs:
$(a_i\ b_j)$ + SIN + CIN.

FA2A (Figure 15) performs:
$(a_{j+1}\ b_0)$ + $(a_j\ b_1)$ + CIN.

FAC (Figure 16) performs:
$((A_{m-j}\ b_{n-1}$ AND TCB) OR $(a_{m-j}\ b_{n-1}$ AND TCB*)) + SIN + CIN, where TCB* is the inverse of TCB.

FACA (Figure 17) performs:
$((a_{m-1}\ B_{n-j}$ AND TCA) OR $(a_{m-1}\ b_{n-j}$ AND TCA*)) + $a_{m-2}\ b_{n-j+1}$ + CIN.

FACC (Figure 18) performs:
$((a_{m-1}\ B_{n-2}$ AND TCA) OR $(a_{m-1}\ b_{n-2}$ AND TCA*)) +
$((A_{m-2}\ b_{n-1}$ AND TCB) OR $(a_{m-2}\ b_{n-1}$ AND TCB*)) + CIN.

FAAC (Figure 19) performs:
$((a_{m-1}\ b_{n-1}$ AND MXM) OR (NOT$(a_{m-1}\ b_{n-1})$ AND MXM*)) +
a_{m-1} TCA + b_{n-1} TCB. Note here that A B+1 is logically equivalent to NOT(A B).

FAAC3 (Figure 20) performs:
$((c_{m+n-1}$ AND TCC) OR $(C_{m+n-1}$ AND TCC*) + A_{m-1} TCA + B_{n-1} TCB.

HAC (Figure 21) performs: TCC + SIN.

HAC2 (Figure 22) performs: A + B.

FAC, FACA, FACC, FAAC, FAAC3 are all adder elements that perform more than one type of addition, and are controlled by signals TCA, TCB, TCC, and MXM. The generation of TCA, TCB, TCC, and MXM is detailed in Figure 24 and in the chart below.

Mode	TCA	TCB	TCC	MXM
Unsigned	0	0	0	0
Mixed Mode B	0	1	0	1
Mixed Mode A	1	0	0	1
Two's Complement	1	1	1	0

The above elements when connected as shown in Figure 12 perform together as a universal multiplier-accumulator, capable of multiplying in unsigned mode, two's complement mode, and mixed modes A and B.

Figure 12b further shows the preferred embodiment having multiple data input bits V_{SS} (logical 0), V_{DD} (logical 1), a_0-a7, b_0-b_7, and carry in bits c_0-c_{15}. Output bits

include carry-out bits c_0-c_{15} and sum bits s_0-s_{16}. MXM, TCA, TCB, and TCC are control inputs, and NC denotes a no-connect. Sum-out and carry-out bits s_0-s_{16} and co_0-co_{15} are summed in final adder 11 of Figure 12a.

Simplicity and interconnectivity are improved by designing similarity across all elements. For example, each full-adder shares the same basic primitive cell (FA1S) with compensation logic included as required. Some adder elements must be able to perform more than one function. It is primarily for this reason that several adder types are used in the preferred embodiment.

For example, element 168 of Figure 12b multiply-accumulates a_7 b_7 in unsigned mode, a_7 b_7+a_7+b_7 in two's complement mode, A_7 B_7+a_7 in mixed mode A, and A_7 B_7+b_7 in mixed mode B (compare Figures 8c, 9c, 10c, and 11c, respectively).

The partial products within term M for all multiplication modes are performed within elements 100-106, 200-206, 300-306, 400-406, 500-506, 600-606, and 700-706. For example, the partial product a_0 b_0 is implemented by FA2A element 100 when connected as shown in Figure 12b.

Term O of Figure 8a is shown in Figure 8b at the upper left side of M. These terms are implemented by elements 107, 117, 127, 137, 147, 157, and 167. For example, term a_7 b_0 in Figure 8b is implemented by element 107 when connected as shown.

Term N of Figures 8a and 8b is implemented by elements 160-166. For example, term a_0 b_7 is implemented by element 160 when connected as shown.

These terms in other modes are similarly accomplished by the preferred embodiment.

Elements **108** and **171** are now further elucidated. Term a_{m-1} is added in the column of c_{m-1} in two's complement mode and mixed mode A. Term b_{n-1} is added in the column of c_{n-1} in two's complement mode and mixed mode B. In the preferred embodiment, **m=n=8**, so **a7** and/or **b7** are added in the column of **c7** in all but unsigned mode. The addition of term a_7 is accomplished by element **108**. Note that **108** outputs a differential signal. The addition of term b_7 is accomplished by element **171**. This arrangement allows proper addition of a_{m-1} and b_{n-1} even if **m=/n**.

Final addition of the sumout and carryout terms of the preferred array **10** is performed by final adder **11**, shown in Figure **12a**, which comprises any of several possible adder configurations, including, for example, full carry look ahead, carry select, and conditional-sum type adders.

The preferred embodiment is fast when fast adders (such as the preferred) are used. Speed is further improved in the preferred embodiment in Figure **12** by summing all even rows together, summing all odd rows together, and adding the even sum with the odd sum in final adder **11** (a Wallace tree technique). It is noted that three or more groups of rows can similarly be summed, but the apparent speed improvement thus gained is lost due to increased parasitic capacitances in the longer interconnections. A path limit of 22 mils or less is deemed desirable to limit parasitics and optimize speed. Short interconnections therefore makes Wallace tree summation of two groups of rows preferable.

Many variations may be made t the embodiment without making it a different invention. Different adder element designs may be used, as well as alternate EXOR designs. Although the preferred embodiment is integrated into a semiconductor substrate using CMOS techniques, other fabrication technologies might be used. The circuit may be constructed discretely and still embody the same invention.

Claims:

1. Apparatus to obtain a product P from terms X and Y and accumulate it with a term Z, the result for use in a digital processing system, wherein P is one of the group $P_{tc}=X_{tc}\ Y_{tc}$, $P_{uns}=X_{uns}\ Y_{uns}$, $P_A=X_{tc}\ Y_{uns}$, and $P_B=X_{uns}\ Y_{tc}$, wherein X is representable as vector $(a_{m-1},a_{m-2},\ldots,a_0)$ and Y as vector $(b_{n-1},b_{n-2},\ldots,b_0)$, comprising:

L means, to form $L = a_{m-1}\ b_{n-1}\ 2^{m+n-2}$;

M means, to form $M = \Sigma\Sigma\ a_i\ b_j\ 2_{i+j}$ for i from 0 to m-2 and j from 0 to n-2;

N means, to form $N = \Sigma\ a_i\ b_{n-1}\ 2^{n-1+i}$ for i from 0 to m-2;

O means, to form $O = \Sigma\ a_{m-1}\ b_j\ 2^{m-1+j}$ for j from 0 to n-2;

compensation means, to form one or more compensations L_{2RC}, N_{2RC}, and O_{2RC}, in the event that one or more of L, N, and O, respectively, are negative;

P means, to form P of one of the group P_{uns}, P_{tc}, P_A, and P_B, wherein P_{uns} is formed by summing L, M, N, and O, P_{tc} is formed by summing L, M, N_{2RC}, and O_{2RC}, P_A is formed by summing L_{2RC}, M, N, and O_{2RC}, and P_B is formed by summing L_{2RC}, M, N_{2RC}, and O; and

accumulation means, to accumulate P with Z;

wherein all summations are done in an interconnected array of substantially identical 3-bit adders arranged in a Wallace tree.

2. Apparatus to form a product P of $X=(a_{m-1}, a_{m-2}, \ldots, a_0)$ and $Y=(b_{n-1}, b_{n-2}, \ldots, b_0)$, and accumulate P with a term Z, wherein the result is for use in a digital processing system, and wherein each of X and Y may be in two's complement mode or in unsigned mode, comprising:

first means, to form terms $a_i\ b_j$ for all i and j yielding positive values;

second means, to form a combination of positive terms equivalent to any combination of terms $a_i\ b_j$ which is negative;

third means, to selectively combine said terms formed by said first means and said combination of positive terms formed by said second means, to form P; and

accumulation means, to accumulate P with Z;

wherein all summations are done in an interconnected array of substantially identical 3-bit adders arranged in a Wallace tree.

3. Apparatus to form a product $P=(p_{m+n-1},p_{m+n-2},\ldots,p_0)$ of $X=(a_{m-1},a_{m-2},\ldots,a_0)$ and $Y=(b_{n-1},b_{n-2},\ldots,b_0)$, and accumulate P with a term Z, wherein the result is for use in a digital processing system, and wherein each of X and Y may be in two's complement mode or in unsigned mode, comprising:

means to complement terms a_i and b_j to obtain terms A_i and B_j, respectively, for $0\leq i\leq m-1$ and $0\leq j\leq n-1$;

means to form terms $a_{m-1}\ b_{n-1}$, $a_i\ b_j$, $a_i\ b_{n-1}$, $A_i\ b_{n-1}$, $a_{m-1}\ b_j$, and $a_{m-1}\ B_j$, for $0\leq i\leq m-2$ and $0\leq j\leq n-2$;

means to form a term which is the complement of said term $a_{m-1}\ b_{n-1}$;

means to form at least one term having the constant value 1; and

means to selectively combine said terms so formed, including:

means to form p_k for $0 \leq k \leq m+n-2$, to form **P** for **X** and **Y** both in unsigned mode, by summing said terms a_i b_j where $i+j=k$, and carries from the sum for k-1;

means to form p_k for $0 \leq k \leq m+n-1$, to form **P** for **X** and **Y** both in two's complement mode,

by adding to the sum for each k for $0 \leq i \leq m-2$ and $0 \leq j \leq n-2$ said terms a_i b_j, a_{m-1}, b_{n-1}, A_i b_{n-1}, a_{m-1} B_j, and a_{m-1} b_{n-1}, wherein the sum of the subscripts within each term is equal to k,

by adding said terms a_{m-1} and b_{n-1} to the sum for $k=m+n-2$,

by adding said terms A_{m-1}, B_{n-1}, and 1 to the sum for $k=m+n-1$, and

by adding carries from the sum for each k-1 to the sum for each k;

means to form p_k for $0 \leq k \leq m+n-1$, to form **P** for **X** in two's complement mode and **Y** in unsigned mode,

by adding to the sum for each k for $0 \leq i \leq m-2$ and $0 \leq j \leq n-2$ said terms a_i b_j, a_{m-1}, a_i b_{n-1}, a_{m-1} B_j, and A_{m-1} B_{n-1}, wherein the sum of the subscripts within each term is equal to k,

by adding said terms a_{m-1} and 1 to the sum for k=m+n-2,

by adding said terms A_{m-1} and 1 to the sum for k=m+n-1, and

by adding carries from the sum for each k-1 to the sum for each k;

means to form p_k for $0 \leq k \leq m+n-1$, to form P for X in unsigned mode and Y in two's complement mode,

by adding to the sum for each k for $0 \leq i \leq m-2$ and $0 \leq j \leq n-2$ said terms $a_i b_j$, b_{n-1}, $A_i b_{n-1}$, $a_{m-1} b_j$, and $A_{m-1} B_{n-1}$, wherein the sum of the subscripts within each term is equal to k,

by adding said terms b_{n-1} and 1 to the sum for k=m+n-2,

by adding said terms B_{n-1} and 1 to the sum for k=m+n-1, and

by adding carries from the sum for each k-1 to the sum for each k; and

accumulation means, to accumulate P with Z;

wherein all summations are done in an interconnected array of substantially identical 3-bit adders arranged in a Wallace tree.

4. Apparatus to obtain a product P and accumulate it with a term Z, the result for use in a digital processing system, wherein P is one of the group $P_{tc}=X_{tc}\ Y_{tc}$, $P_{uns}=X_{uns}\ Y_{uns}$, $P_A=X_{tc}\ Y_{uns}$, and $P_B=X_{uns}\ Y_{tc}$, wherein X is representable as vector $(a_{m-1},a_{m-2},\ldots,a_0)$ and Y as vector $(b_{n-1},b_{n-2},\ldots,b_0)$, comprising:

first means, to form

$L = a_{m-1}\ b_{n-1}\ 2^{m+n-2}$,

$M = \Sigma\Sigma\ a_i\ b_j\ 2_{i+j}$ for i from 0 to m-2 and j from 0 to n-2,

$N = \Sigma\ a_i\ b_{n-1}\ 2^{n-1+i}$ for i from 0 to m-2, and

$O = \Sigma\ a_{m-1}\ b_j\ 2^{m-1+j}$ for j from 0 to n-2;

compensation means, to form one or more compensations L_{2RC}, N_{2RC}, and O_{2RC}, in the event that one or more of L, N, and O, respectively, are negative; and

second means, to form P of one of the group P_{uns}, P_{tc}, P_A, and P_B, wherein P_{uns} is formed by summing L, M, N, and O, P_{tc} is formed by summing L, M, N_{2RC}, and O_{2RC}, P_A is formed by

summing L_{2RC}, M, N, and O_{2RC}, and P_B is formed by summing L_{2RC}, M, N_{2RC}, and ;

third means to select one of the group P_{uns}, P_{tc}, P_A, and P_B, to provide as P; and

accumulation means, to accumulate P with Z;

wherein all summations are done in an interconnected array of substantially identical 3-bit adders arranged in a Wallace tree.

5. Apparatus to obtain a product P for use in a digital processing system, wherein P is one of the group $P_{tc}=X_{tc}\ Y_{tc}$, $P_{uns}=X_{uns}\ Y_{uns}$, $P_A=X_{tc}\ Y_{uns}$, and $P_B=X_{uns}\ Y_{tc}$, wherein X is representable as vector $(a_{m-1},a_{m-2},\ldots,a_0)$ and Y as vector $(b_{n-1},b_{n-2},\ldots,b_0)$, comprising:

L means, to form $L = a_{m-1}\ b_{n-1}\ 2^{m+n-2}$;

M means, to form $M = \Sigma\Sigma\ a_i\ b_j\ 2_{i+j}$ for i from 0 to m-2 and j from 0 to n-2;

N means, to form $N = \Sigma\ a_i\ b_{n-1}\ 2^{n-1+i}$ for i from 0 to m-2;

O means, to form $O = \Sigma\ a_{m-1}\ b_j\ 2^{m-1+j}$ for j from 0 to n-2; and

P means, to form P of one of the group P_{uns}, P_{tc}, P_A, and P_B, wherein P_{uns} is formed by summing L, M, N, and O, P_{tc} is formed by summing L and M and subtracting N and O, P_A is formed by summing M and N and subtracting L and O, and P_B is formed by summing M and O and subtracting L and N.

6. The apparatus of Claim 5, further comprising means within each of said L, N, and O means, to form compensations L_{2RC}, N_{2RC}, and O_{2RC}, respectively, so that any subtraction of L, N, or O within said P means is obtained by a summation of L_{2RC}, N_{2RC}, or O_{2RC}, respectively.

7. Apparatus to obtain a product P for use in a digital processing system, wherein P is one of the group $P_{tc}=X_{tc}\ Y_{tc}$, $P_{uns}=X_{uns}\ Y_{uns}$, $P_A=X_{tc}\ Y_{uns}$, and $P_B=X_{uns}\ Y_{tc}$, wherein X is representable as vector $(a_{m-1},a_{m-2},\ldots,a_0)$ and Y as vector $(b_{n-1},b_{n-2},\ldots,b_0)$, comprising:

L means, to form $L = a_{m-1}\ b_{n-1}\ 2^{m+n-2}$;

M means, to form $M = \Sigma\Sigma\ a_i\ b_j\ 2_{i+j}$ for i from 0 to m-2 and j from 0 to n-2;

N means, to form $N = \Sigma\ a_i\ b_{n-1}\ 2^{n-1+i}$ for i from 0 to m-2;

O means, to form $O = \Sigma\ a_{m-1}\ b_j\ 2^{m-1+j}$ for j from 0 to n-2;

compensation means, to form one or more compensations L_{2RC}, N_{2RC}, and O_{2RC}, in the event that one or more of L, N, and O, respectively, are negative; and

P means, to form P of one of the group P_{uns}, P_{tc}, P_A, and P_B, wherein P_{uns} is formed by summing L, M, N, and O, P_{tc} is formed by summing L, M, N_{2RC}, and O_{2RC}, P_A is formed by summing L_{2RC}, M, N, and O_{2RC}, and P_B is formed by summing L_{2RC}, M, N_{2RC}, and O.

8. Apparatus to form a product P of $X=(a_{m-1},a_{m-2},\ldots,a_0)$ and $Y=(b_{n-1},b_{n-2},\ldots,b_0)$, wherein P is for use in a digital processing system, and wherein each of X and Y may be in two's complement mode or in unsigned mode, comprising:

first means, to form terms a_i b_j for all i and j yielding positive values;

second means, to form a combination of positive terms equivalent to any combination of terms a_i b_j which is negative; and

third means, to selectively combine said terms formed by said first means and said combination of positive terms formed by said second means, to form P.

9. Apparatus to form a product $P=(p_{m+n-1},p_{m+n-2},\ldots,p_0)$ of $X=(a_{m-1},a_{m-2},\ldots,a_0)$ and $Y=(b_{n-1},b_{n-2},\ldots,b_0)$, wherein P is for use in a digital processing system, and wherein each of X and Y may be in two's complement mode or in unsigned mode, comprising:

means to complement terms a_i and b_j to obtain terms A_i and B_j, respectively, for $0\leq i\leq m-1$ and $0\leq j\leq n-1$;

means to form terms $a_{m-1}\ b_{n-1}$, $a_i\ b_j$, $a_i\ b_{n-1}$, $A_i\ b_{n-1}$, $a_{m-1}\ b_j$, and $a_{m-1}\ B_j$, for $0\leq i\leq m-2$ and $0\leq j\leq n-2$;

means to form a term which is the complement of said term $a_{m-1}\ b_{n-1}$;

means to form at least one term having the constant value 1; and

means to selectively combine said terms so formed.

10. The apparatus of Claim 9, wherein, for X and Y both in unsigned mode, said means for selectively combining includes:

means to form p_k for $0\leq k\leq m+n-2$, by summing said terms $a_i\ b_j$ where $i+j=k$, and carries from the sum for k-1.

11. The apparatus of Claim 9, wherein, for X and Y both in two's complement mode, said means for selectively combining includes:

means to form p_k for $0 \leq k \leq m+n-1$,

by adding to the sum for each k for $0 \leq i \leq m-2$ and $0 \leq j \leq n-2$ said terms $a_i b_j$, a_{m-1}, b_{n-1}, $A_i b_{n-1}$, $a_{m-1} B_j$, and $a_{m-1} b_{n-1}$, wherein the sum of the subscripts within each term is equal to k,

by adding said terms a_{m-1} and b_{n-1} to the sum for $k=m+n-2$,

by adding said terms A_{m-1}, B_{n-1}, and 1 to the sum for $k=m+n-1$, and

by adding carries from the sum for each k-1 to the sum for each k.

12. The apparatus of Claim 9, wherein, for X in two's complement mode and Y in unsigned mode, said means for selectively combining includes:

means to form p_k for $0 \leq k \leq m+n-1$,

by adding to the sum for each k for $0 \le i \le m-2$ and $0 \le j \le n-2$ said terms $a_i b_j$, a_{m-1}, $a_i b_{n-1}$, $a_{m-1} B_j$, and $A_{m-1} B_{n-1}$, wherein the sum of the subscripts within each term is equal to k,

by adding said terms a_{m-1} and 1 to the sum for $k=m+n-2$,

by adding said terms A_{m-1} and 1 to the sum for $k=m+n-1$; and

by adding carries from the sum for each k-1 to the sum for each k.

13. The apparatus of Claim 9, wherein, for X in unsigned mode and Y in two's complement mode, said means for selectively combining includes:

means to form p_k for $0 \le k \le m+n-1$,

by adding to the sum for each k for $0 \le i \le m-2$ and $0 \le j \le n-2$ said terms $a_i b_j$, b_{n-1}, $A_i b_{n-1}$, $a_{m-1} b_j$, and $A_{m-1} B_{n-1}$, wherein the sum of the subscripts within each term is equal to k,

by adding said terms b_{n-1} and 1 to the sum for $k=m+n-2$,

by adding said terms B_{n-1} and 1 to the sum for k=m+n-1; and

by adding carries from the sum for each k-1 to the sum for each k.

14. The apparatus of Claim 9, wherein said means for selectively combining includes:

means to form p_k for $0 \leq k \leq m+n-2$, to form P for X and Y both in unsigned mode, by summing said terms a_i b_j where i+j=k, and carries from the sum for k-1;

means to form p_k for $0 \leq k \leq m+n-1$, to form P for X and Y both in two's complement mode,

by adding to the sum for each k for $0 \leq i \leq m-2$ and $0 \leq j \leq n-2$ said terms a_i b_j, a_{m-1}, b_{n-1}, A_i b_{n-1}, a_{m-1} B_j, and a_{m-1} b_{n-1}, wherein the sum of the subscripts within each term is equal to k,

by adding said terms a_{m-1} and b_{n-1} to the sum for k=m+n-2,

by adding said terms A_{m-1}, B_{n-1}, and 1 to the sum for k=m+n-1, and

by adding carries from the sum for each k-1 to the sum for each k;

means to form p_k for $0 \le k \le m+n-1$, to form P for X in two's complement mode and Y in unsigned mode,

by adding to the sum for each k for $0 \le i \le m-2$ and $0 \le j \le n-2$ said terms $a_i b_j$, a_{m-1}, $a_i b_{n-1}$, $a_{m-1} B_j$, and $A_{m-1} B_{n-1}$, wherein the sum of the subscripts within each term is equal to k,

by adding said terms a_{m-1} and 1 to the sum for $k=m+n-2$,

by adding said terms A_{m-1} and 1 to the sum for $k=m+n-1$, and

by adding carries from the sum for each k-1 to the sum for each k;

means to form p_k for $0 \le k \le m+n-1$, to form P for X in unsigned mode and Y in two's complement mode,

by adding to the sum for each k for $0 \le i \le m-2$ and $0 \le j \le n-2$ said terms $a_i b_j$, b_{n-1}, $A_i b_{n-1}$, $a_{m-1} b_j$, and $A_{m-1} B_{n-1}$, wherein the sum of the subscripts within each term is equal to k,

by adding said terms b_{n-1} and 1 to the sum for $k=m+n-2$,

by adding said terms B_{n-1} and 1 to the sum for k=m+n-1; and

by adding carries from the sum for each k-1 to the sum for each k.

15. Apparatus to obtain a product P for use in a digital processing system, wherein P is one of the group $P_{tc}=X_{tc}\ Y_{tc}$, $P_{uns}=X_{uns}\ Y_{uns}$, $P_A=X_{tc}\ Y_{uns}$, and $P_B=X_{uns}\ Y_{tc}$, wherein X is representable as vector $(a_{m-1},a_{m-2},\ldots,a_0)$ and Y as vector $(b_{n-1},b_{n-2},\ldots,b_0)$, comprising:

first means, to form

$L = a_{m-1}\ b_{n-1}\ 2^{m+n-2}$,

$M = \Sigma\Sigma\ a_i\ b_j\ 2_{i+j}$ for i from 0 to m-2 and j from 0 to n-2,

$N = \Sigma\ a_i\ b_{n-1}\ 2^{n-1+i}$ for i from 0 to m-2, and

$O = \Sigma\ a_{m-1}\ b_j\ 2^{m-1+j}$ for j from 0 to n-2;

second means, to form P_{uns}, P_{tc}, P_A, and P_B, wherein P_{uns} is formed by summing L, M, N, and O, P_{tc} is formed by summing L and M and subtracting N and O, P_A is formed by summing M and N and subtracting L and O, and P_B is formed by summing M and O and subtracting L and N; and

third means, to select one of the group P_{uns}, P_{tc}, P_A, and P_B, to provide as P.

16. The apparatus of Claim 15, which further comprises means within each of said L, N, and O means, to form compensations L_{2RC}, N_{2RC}, and O_{2RC}, respectively, so that any subtraction of L, N, or O within said second means is obtained by a summation of L_{2RC}, N_{2RC}, or O_{2RC}, respectively.

17. Apparatus to obtain a product P for use in a digital processing system, wherein P is one of the group $P_{tc}=X_{tc}\ Y_{tc}$, $P_{uns}=X_{uns}\ Y_{uns}$, $P_A=X_{tc}\ Y_{uns}$, and $P_B=X_{uns}\ Y_{tc}$, wherein X is representable as vector $(a_{m-1},a_{m-2},\ldots,a_0)$ and Y as vector $(b_{n-1},b_{n-2},\ldots,b_0)$, comprising:

first means, to form

$L = a_{m-1}\ b_{n-1}\ 2^{m+n-2}$,

$M = \Sigma\Sigma\ a_i\ b_j\ 2_{i+j}$ for i from 0 to m-2 and j from 0 to n-2,

$N = \Sigma\ a_i\ b_{n-1}\ 2^{n-1+i}$ for i from 0 to m-2, and

$O = \Sigma\ a_{m-1}\ b_j\ 2^{m-1+j}$ for j from 0 to n-2;

compensation means, to form one or more compensations L_{2RC}, N_{2RC}, and O_{2RC}, in the event that one or more of L, N, and O, respectively, are negative; and

second means, to form P of one of the group P_{uns}, P_{tc}, P_A, and P_B, wherein P_{uns} is formed by summing L, M, N, and O, P_{tc} is formed by summing L, M, N_{2RC}, and O_{2RC}, P_A is formed by summing L_{2RC}, M, N, and O_{2RC}, and P_B is formed by summing L_{2RC}, M, N_{2RC}, and O; and

third means to select one of the group P_{uns}, P_{tc}, P_A, and P_B, to provide as P.

18. The apparatus of Claim 17, which further comprises accumulation means, to accumulate P with an accumulation term Z.

19. The apparatus of Claims 1, 2, 3, 4, 5, 7, 8, 14, 15 or 17, wherein at least one of said substantially identical 3-bit adders includes:

a sum generator, comprising:

first and second XOR means;

first and second inputs of said first XOR means being differentially responsive to first and second bits, respectively, and first and second inputs of said second XOR means being differentially responsive to an

output of said first XOR means, and a third bit, respectively;

wherein an output of said second XOR means is able to provide a differential output for the sum generator, having a first state when an odd subset of said first, second, and third bits are true, and having a second state when an even subset of said first, second, and third bits are true;

wherein at least one of said first and second XOR means comprises:

first, second, third, and fourth tristate means;

an input of each of said tristate means being inputs W, X, Y, and Z, respectively, of the XOR means;

an output of each of said first and second tristate means being connected together to form a first XOR means output;

an output of each of said third and fourth tristate means being connected together to form a second XOR means output; and

said first and third tristate means being tristated when an enable input is in a first state, and said second and fourth tristate means being tristated when said enable input is in a second state;

wherein said inputs W and Z are responsive together and said inputs X and Y are responsive together, said inputs W and X are differentially responsive to a bit A, said enable input is differentially responsive to a bit B, and said first and second logic circuit outputs are able to differentially provide an XOR function of said bits A and B;

a carry-out generator, comprising:

a first input, responsive to said output of said first XOR means;

a second input, differentially responsive to one of said first and second bits;

a third input, differentially responsive to said third bit; and

logic means, able to provide a first differential state when at least two of said first, second, and

third bits are true, and otherwise able to provide a second state;

wherein said sum generator and said carry-out generator are able to provide a sum bit and a carry-out bit, respectively, on said first, second, and third bits;

wherein said logic means comprises:

first, second, third, and fourth tristate means;

an input of each of said tristate means being inputs W, X, Y, and Z, respectively, of the logic means;

an output of each of said first and second tristate means being connected together to form a first logic means output;

an output of each of said third and fourth tristate means being connected together to form a second logic means output; and

said first and third tristate means being tristated when an enable input is in a first state, and said second and fourth tristate means

being tristated when said enable input is in a second state;

wherein said enable input is said first input, said inputs X and Z form said second input, and said inputs W and Y form said third input;

wherein said sum generator and said carry-out generator are able to provide a sum bit and a carry-out bit, respectively, on said first, second, and third bits.

20. The apparatus of Claims 5, 7, 8, 9, or 15, which further comprises accumulation means, to accumulate P with an accumulation term Z.

21. The apparatus of Claims 5, 7, 8, 9, 15, or 17, wherein all summations are done in an interconnected array of substantially identical adders.

22. The apparatus of Claims 5, 7, 8, 9, 15, or 17, wherein said substantially identical adders comprise 3-bit adders.

23. The apparatus of Claims 5, 7, 8, 9, 15 or 17, wherein all summations are done using a Wallace tree technique.

24. A multiplier-accumulator array, having adders comprising:

a sum generator, comprising:

first and second XOR means;

first and second inputs of said first XOR means being differentially responsive to first and second bits, respectively, and first and second inputs of said second XOR means being differentially responsive to an output of said first XOR means, and a third bit, respectively;

wherein an output of said second XOR means is able to provide a differential output for the sum generator, having a first state when an odd subset of said first, second, and third bits are true, and having a second state when an even subset of said first, second, and third bits are true;

wherein at least one of said first and second XOR means comprises:

first, second, third, and fourth tristate means;

an input of each of said tristate means being inputs W, X, Y, and Z, respectively, of the XOR means;

an output of each of said first and second tristate means being connected together to form a first XOR means output;

an output of each of said third and fourth tristate means being connected together to form a second XOR means output; and

said first and third tristate means being tristated when an enable input is in a first state, and said second and fourth tristate means being tristated when said enable input is in a second state;

wherein said inputs W and Z are responsive together and said inputs X and Y are responsive together, said inputs W and X are differentially responsive to a bit A, said enable input is differentially responsive to a bit B, and said first and second logic circuit outputs are able to differentially provide an XOR function of said bits A and B;

a carry-out generator, comprising:

a first input, responsive to said output of said first XOR means;

a second input, differentially responsive to one of said first and second bits;

a third input, differentially responsive to said third bit; and

logic means, able to provide a first differential state when at least two of said first, second, and third bits are true, and otherwise able to provide a second state;

wherein said sum generator and said carry-out generator are able to provide a sum bit and a carry-out bit, respectively, on said first, second, and third bits;

wherein said logic means comprises:

first, second, third, and fourth tristate means;

an input of each of said tristate means being inputs W, X, Y, and Z, respectively, of the logic means;

an output of each of said first and second tristate means being connected together to form a first logic means output;

an output of each of said third and fourth tristate means being connected together to form a second logic means output; and

said first and third tristate means being tristated when an enable input is in a first state, and said second and fourth tristate means being tristated when said enable input is in a second state;

wherein said enable input is said first input, said inputs X and Z form said second input, and said inputs W and Y form said third input;

wherein said sum generator and said carry-out generator are able to provide a sum bit and a carry-out bit, respectively, on said first, second, and third bits.

25. The apparatus of Claims 5, 7, 8, 9, 15, 17, or 24, wherein said adders are arranged in a Wallace tree.

26. A machine method to obtain a product P from terms X and Y and accumulate it with a term Z, the result for use

in a digital processing system, wherein P is on of the group $P_{tc}=X_{tc}\ Y_{tc}$, $P_{uns}=X_{uns}\ Y_{uns}$, $P_A=X_{tc}\ Y_{uns}$, and $P_B=X_{uns}\ Y_{tc}$, wherein X is representable as vector $(a_{m-1},a_{m-2},\ldots,a_0)$ and Y as vector $(b_{n-1},b_{n-2},\ldots,b_0)$, comprising the steps of:

forming $L = a_{m-1}\ b_{n-1}\ 2^{m+n-2}$;

forming $M = \Sigma\Sigma\ a_i\ b_j\ 2_{i+j}$ for i from 0 to m-2 and j from 0 to n-2;

forming $N = \Sigma\ a_i\ b_{n-1}\ 2^{n-1+i}$ for i from 0 to m-2;

forming $O = \Sigma\ a_{m-1}\ b_j\ 2^{m-1+j}$ for j from 0 to n-2;

forming one or more compensations L_{2RC}, N_{2RC}, and O_{2RC}, in the event that one or more of L, N, and O, respectively, are negative;

forming P of one of the group P_{uns}, P_{tc}, P_A, and P_B, wherein P_{uns} is formed by summing L, M, N, and O, P_{tc} is formed by summing L, M, N_{2RC}, and O_{2RC}, P_A is formed by summing L_{2RC}, M, N, and O_{2RC}, and P_B is formed by summing L_{2RC}, M, N_{2RC}, and O; and

accumulating P with Z.

27. A machine method to form a product P of $X=(a_{m-1},a_{m-2},\ldots,a_0)$ and $Y=(b_{n-1},b_{n-2},\ldots,b_0)$, and accumulate P with a term Z, wherein the result is for use in a digital processing system, and wherein each of X and Y may be in two's complement mode or in unsigned mode, comprising the steps of:

forming terms $a_i\ b_j$ for all i and j yielding positive values;

forming a combination of positive terms equivalent to any combination of terms $a_i\ b_j$ which is negative;

selectively combining said terms and said combination of positive terms to form P; and

accumulating P with Z.

28. A machine method to form a product $P=(p_{m+n-1},p_{m+n-2},\ldots,p_0)$ of $X=(a_{m-1},a_{m-2},\ldots,a_0)$ and $Y=(b_{n-1},b_{n-2},\ldots,b_0)$, and accumulate P with a term Z, wherein the result is for use in a digital processing system, and wherein each of X and Y may be in two's complement mode or in unsigned mode, comprising the steps of:

providing complement terms A_i and B_j, respectively, for $0\le i\le m-1$ and $0\le j\le n-1$;

providing terms a_{m-1} b_{n-1}, a_i b_j, a_i b_{n-1}, A_i b_{n-1}, a_{m-1} b_j, and a_{m-1} B_j, for $0 \leq i \leq m-2$ and $0 \leq j \leq n-2$;

providing a term which is the complement of said term a_{m-1} b_{n-1};

providing at least one term having the constant value 1; and

selectively combining said terms so formed, including:

forming p_k for $0 \leq k \leq m+n-2$, to form P for X and Y both in unsigned mode, by summing said terms a_i b_j where $i+j=k$, and carries from the sum for k-1;

forming p_k for $0 \leq k \leq m+n-1$, to form P for X and Y both in two's complement mode,

by adding to the sum for each k for $0 \leq i \leq m-2$ and $0 \leq j \leq n-2$ said terms a_i b_j, a_{m-1}, b_{n-1}, A_i b_{n-1}, a_{m-1} B_j, and a_{m-1} b_{n-1}, wherein the sum of the subscripts within each term is equal to k,

by adding said terms a_{m-1} and b_{n-1} to the sum for $k=m+n-2$,

by adding said terms A_{m-1}, B_{n-1}, and 1 to the sum for $k=m+n-1$, and

by adding carries from the sum for each k-1 to the sum for each k;

forming p_k for $0 \leq k \leq m+n-1$, to form P for X in two's complement mode and Y in unsigned mode,

by adding to the sum for each k for $0 \leq i \leq m-2$ and $0 \leq j \leq n-2$ said terms $a_i b_j$, a_{m-1}, $a_i b_{n-1}$, $a_{m-1} B_j$, and $A_{m-1} B_{n-1}$, wherein the sum of the subscripts within each term is equal to k,

by adding said terms a_{m-1} and 1 to the sum for $k=m+n-2$,

by adding said terms A_{m-1} and 1 to the sum for $k=m+n-1$, and

by adding carries from the sum for each k-1 to the sum for each k;

forming p_k for $0 \leq k \leq m+n-1$, to form P for X in unsigned mode and Y in two's complement mode,

by adding to the sum for each k for $0 \leq i \leq m-2$ and $0 \leq j \leq n-2$ said terms $a_i b_j$, b_{n-1}, $A_i b_{n-1}$, $a_{m-1} b_j$, and $A_{m-1} B_{n-1}$, wherein the sum of the subscripts within each term is equal to k,

by adding said terms b_{n-1} and 1 to the sum for k=m+n-2,

by adding said terms B_{n-1} and 1 to the sum for k=m+n-1, and

by adding carries from the sum for each k-1 to the sum for each k; and

accumulating P with Z.

29. A machine method to obtain a product P and accumulate it with a term Z, the result for use in a digital processing system, wherein P is one of the group $P_{tc}=X_{tc}\ Y_{tc}$, $P_{uns}=X_{uns}\ Y_{uns}$, $P_A=X_{tc}\ Y_{uns}$, and $P_B=X_{uns}\ Y_{tc}$, wherein X is representable as vector $(a_{m-1},a_{m-2},\ldots,a_0)$ and Y as vector $(b_{n-1},b_{n-2},\ldots,b_0)$, comprising the steps of:

forming

$L = a_{m-1}\ b_{n-1}\ 2^{m+n-2}$,

$M = \Sigma\Sigma\ a_i\ b_j\ 2_{i+j}$ for i from 0 to m-2 and j from 0 to n-2,

$N = \Sigma\ a_i\ b_{n-1}\ 2^{n-1+i}$ for i from 0 to m-2, and

$O = \Sigma\ a_{m-1}\ b_j\ 2^{m-1+j}$ for j from 0 to n-2;

forming one or more compensations L_{2RC}, N_{2RC}, and O_{2RC}, in the event that one or more of L, N, and O, respectively, are negative; and

forming P of one of the group P_{uns}, P_{tc}, P_A, and P_B, wherein P_{uns} is formed by summing L, M, N, and O, P_{tc} is formed by summing L, M, N_{2RC}, and O_{2RC}, P_A is formed by summing L_{2RC}, M, N, and O_{2RC}, and P_B is formed by summing L_{2RC}, M, N_{2RC}, and O;

selecting one of the group P_{uns}, P_{tc}, P_A, and P_B, to provide as P; and

accumulating P with Z.

$$X = \sum_{i=0}^{m-1} a_i 2^i$$

FIG. 1a

$$Y = \sum_{j=0}^{n-1} b_j 2^j$$

FIG. 1b

$$Z = \sum_{i=0}^{m+n-1} c_i 2^i$$

FIG. 1c

$$X_{tc} = -a_{m-1}2^{m-1} + \sum_{i=0}^{m-2} a_i 2^i$$ FIG. 2a

$$Y_{tc} = -b_{n-1}2^{n-1} + \sum_{j=0}^{n-2} b_j 2^j$$ FIG. 2b

$$Z_{tc} = -c_{m+n-1}2^{m+n-1} + \sum_{i=0}^{m+n-2} c_i 2^i$$ FIG. 2c

$$X_{uns} = a_{m-1}2^{m-1} + \sum_{i=0}^{m-2} a_i 2^i$$ FIG. 2d

$$Y_{uns} = b_{n-1}2^{n-1} + \sum_{j=0}^{n-2} b_j 2^j$$ FIG. 2e

$$Z_{uns} = c_{m+n-1}2^{m+n-1} + \sum_{i=0}^{m+n-2} c_i 2^i$$ FIG. 2f

$$P_{tc} = \underbrace{+a_{m-1}b_{n-1}2^{m+n-2}}_{L} \underbrace{+\sum_{i=0}^{m-2}\sum_{j=0}^{n-2} a_i b_j 2^{i+j}}_{M} \underbrace{-\sum_{i=0}^{m-2} a_i b_{n-1} 2^{n-1+i}}_{N} \underbrace{-\sum_{j=0}^{n-2} a_{m-1} b_j 2^{m-1+j}}_{O}$$

FIG. 3a

$$P_{uns} = +a_{m-1}b_{n-1}2^{m+n-2} + \sum_{i=0}^{m-2}\sum_{j=0}^{n-2} a_i b_j 2^{i+j} + \sum_{i=0}^{m-2} a_i b_{n-1} 2^{n-1+i} + \sum_{j=0}^{n-2} a_{m-1} b_j 2^{m-1+j}$$

FIG. 3b

$$P_A = -a_{m-1}b_{n-1}2^{m+n-2} + \sum_{i=0}^{m-2}\sum_{j=0}^{n-2} a_i b_j 2^{i+j} + \sum_{i=0}^{m-2} a_i b_{n-1} 2^{n-1+i} - \sum_{j=0}^{n-2} a_{m-1} b_j 2^{m-1+j}$$

FIG. 3c

$$P_B = -a_{m-1}b_{n-1}2^{m+n-2} + \sum_{i=0}^{m-2}\sum_{j=0}^{n-2} a_i b_j 2^{i+j} - \sum_{i=0}^{m-2} a_i b_{n-1} 2^{n-1+i} + \sum_{j=0}^{n-2} a_{m-1} b_j 2^{m-1+j}$$

FIG. 3d

$$L = a_{m-1}b_{n-1}2^{m+n-2}$$

$$\left\{ \begin{matrix} 0\cdot 2^{m+n} \\ 0\cdot 2^{m+n-1} \end{matrix} \right. + a_{m-1}b_{n-1}2^{m+n-2} + 0\cdot 2^{m+n-3} + \ldots + 0\cdot 2^{0}$$

FIG. 4a

$$\left\{ \begin{matrix} 1\cdot 2^{m+n} \\ 1\cdot 2^{m+n-1} \end{matrix} \right. + \overline{a_{m-1}b_{n-1}}2^{m+n-2} + 1\cdot 2^{m+n-3} + \ldots + 1\cdot 2^{0}$$

FIG. 4b

$$\left\{ \begin{matrix} 1\cdot 2^{m+n} \\ 1\cdot 2^{m+n-1} \end{matrix} \right. + \overline{a_{m-1}b_{n-1}}2^{m+n-2} + 0\cdot 2^{m+n-3} + \ldots + 0\cdot 2^{0}$$

FIG. 4c

$$\begin{bmatrix} 0 \\ 1 \end{bmatrix} \begin{matrix} 0 \\ 1 \end{matrix} \overline{a_{m-1}b_{n-1}} \begin{matrix} 0 \\ 0 \end{matrix} \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

FIG. 4d

FIG. 4e

$$N = \sum_{i=0}^{m-2} a_i b_{n-1} 2^{n-1+i}$$

FIG. 5a

$$0 \cdot 2^{m+n} + 0 \cdot 2^{m+n-1} + 0 \cdot 2^{m+n-2} + \sum_{i=0}^{m-2} a_i b_{n-1} 2^{n-1+i}$$

FIG. 5b

$$0 \cdot 2^{m+n} + 0 \cdot 2^{m+n-1} + 0 \cdot 2^{m+n-2} + \sum_{i=0}^{m-2} a_i 2^{n-1+i}$$

FIG. 5c

$$1 \cdot 2^{m+n} + 1 \cdot 2^{m+n-1} + 1 \cdot 2^{m+n-2} + 1 + \sum_{i=0}^{m-2} \overline{a_i} 2^{n-1+i}$$

FIG. 5d

$$1 \cdot 2^{m+n} + 1 \cdot 2^{m+n-1} + \overline{b_{n-1}} 2^{m+n-1} + b_{n-1} 2^{m+n-2} + b_{n-1} + \sum_{i=0}^{m-2} \overline{a_i} b_{n-1} 2^{n-1+i}$$

FIG. 5e

$$\begin{bmatrix} 0 & \overline{b_{n-1}} & b_{n-1} & \overline{a_{m-2}} b_{n-1} & \overline{a_{m-3}} b_{n-1} & \cdots & \overline{a_1} b_{n-1} & \overline{a_0} b_{n-1} \\ 1 & 1 & 0 & 0 & 0 & \cdots & 0 & b_{n-1} \end{bmatrix}$$

FIG. 5f

$$O = \sum_{j=0}^{n-2} a_{m-1} b_j 2^{m-1+j}$$ FIG. 6a

$$0 \cdot 2^{m+n} + 0 \cdot 2^{m+n-1} + 0 \cdot 2^{m+n-2} + \sum_{j=0}^{n-2} a_{m-1} b_j 2^{m-1+j}$$ FIG. 6b

$$0 \cdot 2^{m+n} + 0 \cdot 2^{m+n-1} + 0 \cdot 2^{m+n-2} + \sum_{j=0}^{n-2} b_j 2^{m-1+j}$$ FIG. 6c

$$1 \cdot 2^{m+n} + 1 \cdot 2^{m+n-1} + 1 \cdot 2^{m+n-2} + 1 + \sum_{j=0}^{n-2} \overline{b_j} 2^{m-1+j}$$ FIG. 6d

$$1 \cdot 2^{m+n} + 1 \cdot 2^{m+n-1} + \overline{a_{m-1}} 2^{m+n-1} + a_{m-1} 2^{m+n-2} + a_{m-1} + \sum_{j=0}^{n-2} a_{m-1} \overline{b_j} 2^{m-1+j}$$ FIG. 6e

$$\begin{bmatrix} 0 & \overline{a_{m-1}} & a_{m-1} & a_{m-1}\overline{b_{n-2}} & a_{m-1}\overline{b_{n-3}} & \cdots & a_{m-1}\overline{b_1} & a_{m-1}\overline{b_0} \\ 1 & 1 & 0 & 0 & 0 & \cdots & 0 & a_{m-1} \end{bmatrix}$$ FIG. 6f

$$Z_{tc} = -c_{m+n-1}\,2^{m+n-1} + \sum_{i=0}^{m+n-2} c_i 2^i$$

FIG. 7a

$$c_{m+n-1}\,2^{m+n-1} = 0{\cdot}2^{m+n} + c_{m+n-1}\,2^{m+n-1} + 0{\cdot}2^{m+n-2} + \ldots + 0{\cdot}2^0$$

FIG. 7b

$$-c_{m+n-1}\,2^{m+n-1} = 1{\cdot}2^{m+n} + \overline{c_{m+n-1}}\,2^{m+n-1} + 1{\cdot}2^{m+n-2} + \ldots + 1{\cdot}2^0 + 1$$

FIG. 7c

$$-c_{m+n-1}\,2^{m+n-1} = 1{\cdot}2^{m+n} + \overline{c_{m+n-1}}\,2^{m+n-1} + 1{\cdot}2^{m+n-1} + 0{\cdot}2^{m+n-2} + \ldots + 0{\cdot}2^0$$

FIG. 7d

$$\begin{bmatrix} 0 \\ 1 \end{bmatrix} \qquad \begin{matrix} \overline{c_{m+n-1}} & 0 & \cdots & 0 \\ 1 & 0 & \cdots & 0 \end{matrix}$$

FIG. 7e

FIG. 8a

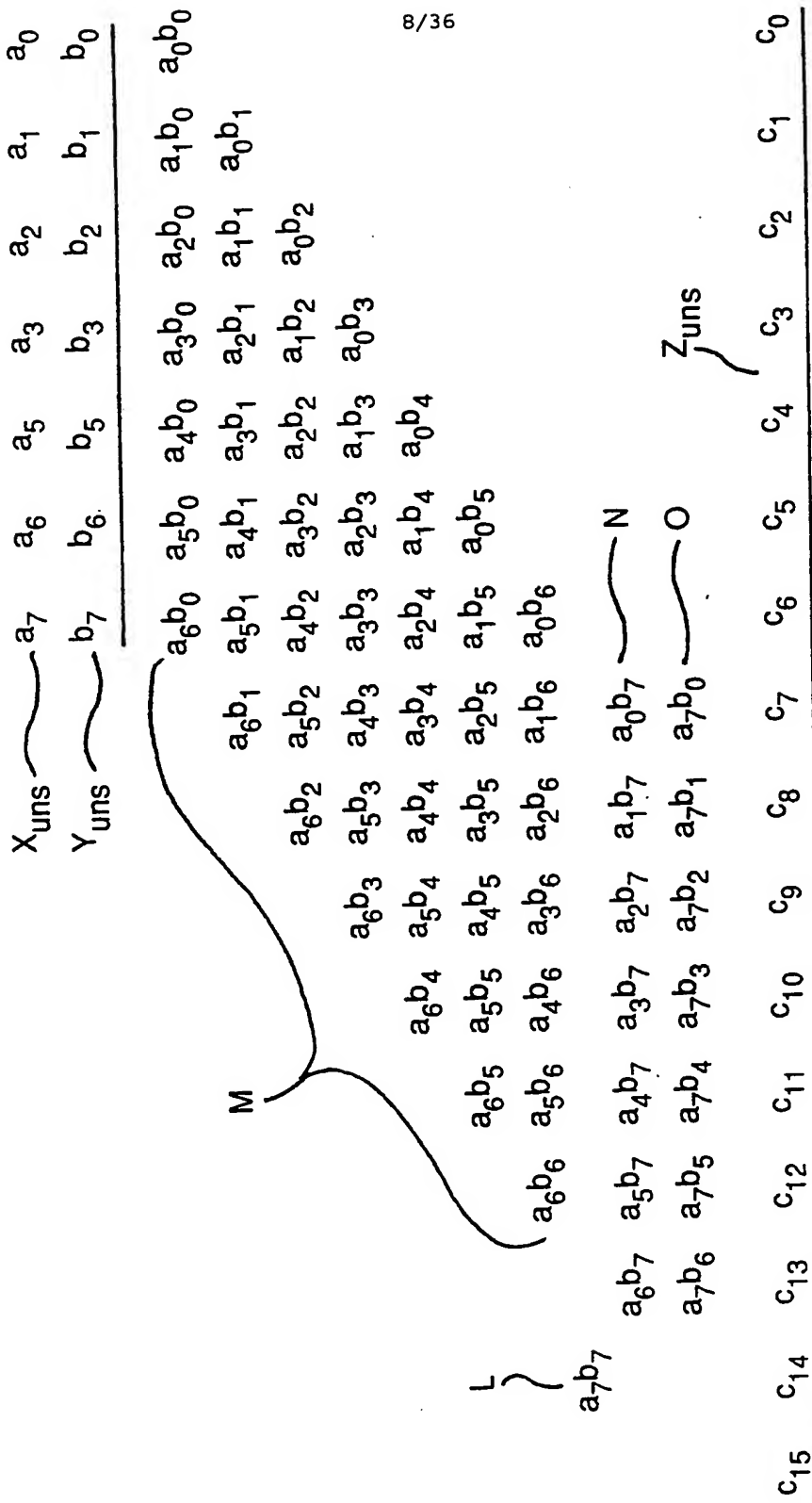

X_{uns} a_7 a_6 a_5 a_3 a_2 a_1 a_0
Y_{uns} b_7 b_6 b_5 b_3 b_2 b_1 b_0
a_6b_0 a_5b_0 a_4b_0 a_3b_0 a_2b_0 a_1b_0 a_0b_0
a_6b_1 a_5b_1 a_4b_1 a_3b_1 a_2b_1 a_1b_1 a_0b_1
a_6b_2 a_5b_2 a_4b_2 a_3b_2 a_2b_2 a_1b_2 a_0b_2
a_6b_3 a_5b_3 a_4b_3 a_3b_3 a_2b_3 a_1b_3 a_0b_3
a_6b_4 a_5b_4 a_4b_4 a_3b_4 a_2b_4 a_1b_4 a_0b_4
a_6b_5 a_5b_5 a_4b_5 a_3b_5 a_2b_5 a_1b_5 a_0b_5
a_6b_6 a_5b_6 a_4b_6 a_3b_6 a_2b_6 a_1b_6 a_0b_6
M
L
a_7b_7
a_6b_7 a_5b_7 a_4b_7 a_3b_7 a_2b_7 a_1b_7 a_0b_7
N
a_7b_6 a_7b_5 a_7b_4 a_7b_3 a_7b_2 a_7b_1 a_7b_0
O
Z_{uns}
c_{15} c_{14} c_{13} c_{12} c_{11} c_{10} c_9 c_8 c_7 c_6 c_5 c_4 c_3 c_2 c_1 c_0

FIG. 8b

						a_7	a_6	a_5	a_3	a_2	a_1	a_0			
						b_7	b_6	b_5	b_3	b_2	b_1	b_0			
						a_6b_0	a_5b_0	a_4b_0	a_3b_0	a_2b_0	a_1b_0	a_0b_0			
					a_7b_0	a_6b_1	a_5b_1	a_4b_1	a_3b_1	a_2b_1	a_1b_1	a_0b_1			
				a_7b_1	a_6b_2	a_5b_2	a_4b_2	a_3b_2	a_2b_2	a_1b_2	a_0b_2				
			a_7b_2	a_6b_3	a_5b_3	a_4b_3	a_3b_3	a_2b_3	a_1b_3	a_0b_3					
		a_7b_3	a_6b_4	a_5b_4	a_4b_4	a_3b_4	a_2b_4	a_1b_4	a_0b_4						
	a_7b_4	a_6b_5	a_5b_5	a_4b_5	a_3b_5	a_2b_5	a_1b_5	a_0b_5							
a_7b_5	a_6b_6	a_5b_6	a_4b_6	a_3b_6	a_2b_6	a_1b_6	a_0b_6								
a_7b_6	a_6b_7	a_5b_7	a_4b_7	a_3b_7	a_2b_7	a_1b_7	a_0b_7								
a_7b_7															
c_{15}	c_{14}	c_{13}	c_{12}	c_{11}	c_{10}	c_9	c_8	c_7	c_6	c_5	c_4	c_3	c_2	c_1	c_0

FIG. 8c

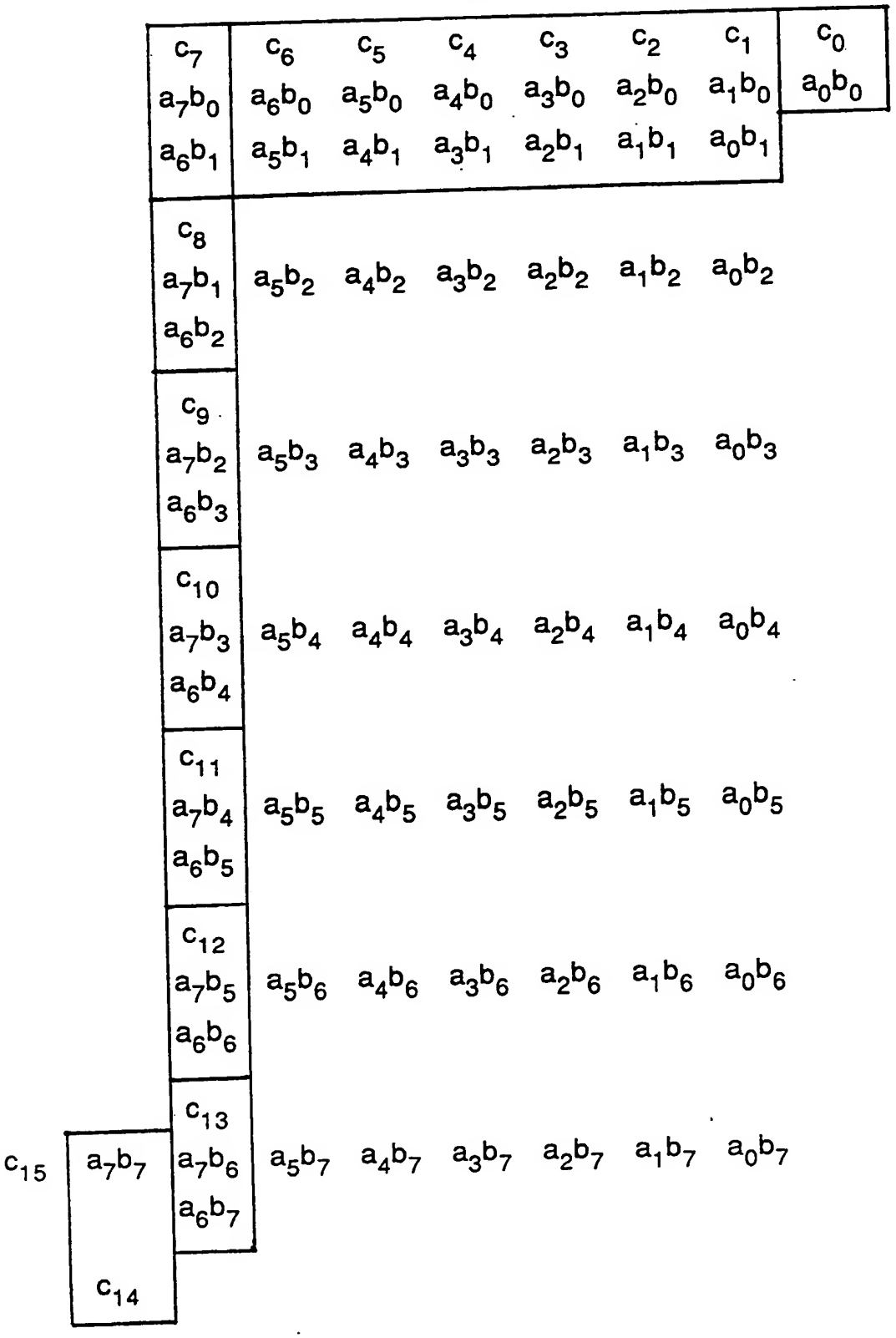
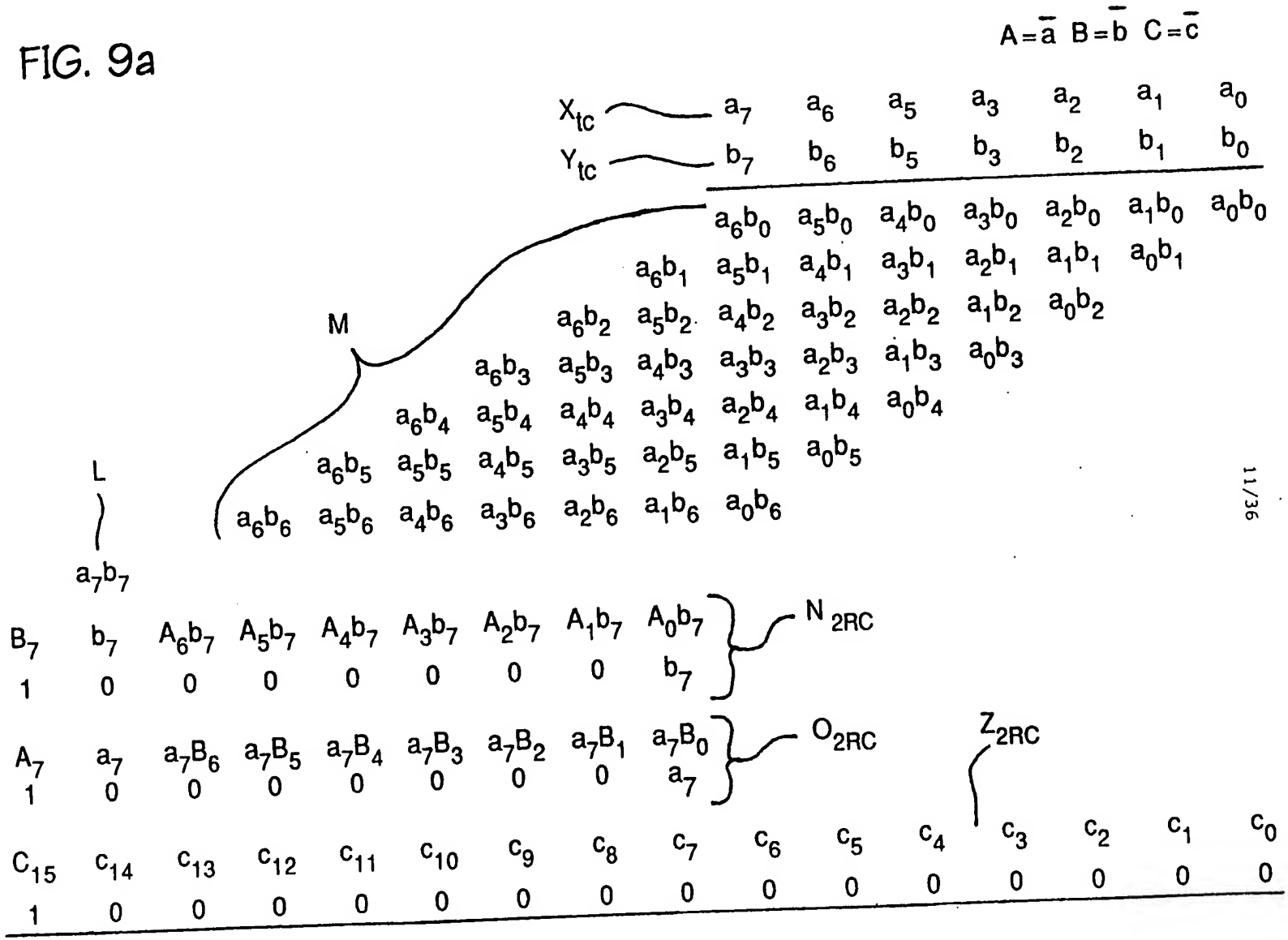

c7 a7b0 a6b1
c6 a6b0 a5b1
c5 a5b0 a4b1
c4 a4b0 a3b1
c3 a3b0 a2b1
c2 a2b0 a1b1
c1 a1b0 a0b1
c0 a0b0
c8 a7b1 a6b2
a5b2 a4b2 a3b2 a2b2 a1b2 a0b2
c9 a7b2 a6b3
a5b3 a4b3 a3b3 a2b3 a1b3 a0b3
c10 a7b3 a6b4
a5b4 a4b4 a3b4 a2b4 a1b4 a0b4
c11 a7b4 a6b5
a5b5 a4b5 a3b5 a2b5 a1b5 a0b5
c12 a7b5 a6b6
a5b6 a4b6 a3b6 a2b6 a1b6 a0b6
c13 a7b6 a6b7
a5b7 a4b7 a3b7 a2b7 a1b7 a0b7
c15 a7b7
c14

FIG. 9a



SUBSTITUTE SHEET

FIG. 9b

$A=\overline{a}\ B=b\ \overline{C}=\overline{c}$

								a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0
								b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
								a_6b_0	a_5b_0	a_4b_0	a_3b_0	a_2b_0	a_1b_0	a_0b_0	
							a_7B_0	a_6b_1	a_5b_1	a_4b_1	a_3b_1	a_2b_1	a_1b_1	a_0b_1	
						a_7B_1	a_6b_2	a_5b_2	a_4b_2	a_3b_2	a_2b_2	a_1b_2	a_0b_2		
					a_7B_2	a_6b_3	a_5b_3	a_4b_3	a_3b_3	a_2b_3	a_1b_3	a_0b_3			
				a_7B_3	a_6b_4	a_5b_4	a_4b_4	a_3b_4	a_2b_4	a_1b_4	a_0b_4				
			a_7B_4	a_6b_5	a_5b_5	a_4b_5	a_3b_5	a_2b_5	a_1b_5	a_0b_5					
		a_7B_5	a_6b_6	a_5b_6	a_4b_6	a_3b_6	a_2b_6	a_1b_6	a_0b_6						
1	a_7b_7	a_7B_6	a_6b_6	a_5b_6	a_4b_6	a_3b_6	a_2b_6	A_1b_7	A_0b_7						
B_7	b_7	A_6b_7	A_5b_7	A_4b_7	A_3b_7	A_2b_7			b_7						
A_7	a_7								a_7						
C_{15}	C_{14}	C_{13}	C_{12}	C_{11}	C_{10}	C_9	C_8	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0

FIG. 9c

$A=\bar{a}$ $B=\bar{b}$ $C=\bar{c}$

c_7 a_7B_0 a_6b_1	c_6 a_6b_0 a_5b_1	c_5 a_5b_0 a_4b_1	c_4 a_4b_0 a_3b_1	c_3 a_3b_0 a_2b_1	c_2 a_2b_0 a_1b_1	c_1 a_1b_0 a_0b_1	c_0 a_0b_0
c_8 a_7B_1 a_6b_2	a_5b_2 a_7	a_4b_2	a_3b_2	a_2b_2	a_1b_2	a_0b_2	
c_9 a_7B_2 a_6b_3	a_5b_3	a_4b_3	a_3b_3	a_2b_3	a_1b_3	a_0b_3	
c_{10} a_7B_3 a_6b_4	a_5b_4	a_4b_4	a_3b_4	a_2b_4	a_1b_4	a_0b_4	
c_{11} a_7B_4 a_6b_5	a_5b_5	a_4b_5	a_3b_5	a_2b_5	a_1b_5	a_0b_5	
c_{12} a_7B_5 a_6b_6	a_5b_6	a_4b_6	a_3b_6	a_2b_6	a_1b_6	a_0b_6	
c_{13} a_7B_6 A_6b_7	A_5b_7	A_4b_7	A_3b_7	A_2b_7	A_1b_7	A_0b_7 b_7	

C_{15} A_7 B_7	a_7b_7 a_7 b_7
1	c_{14}

FIG. 10a

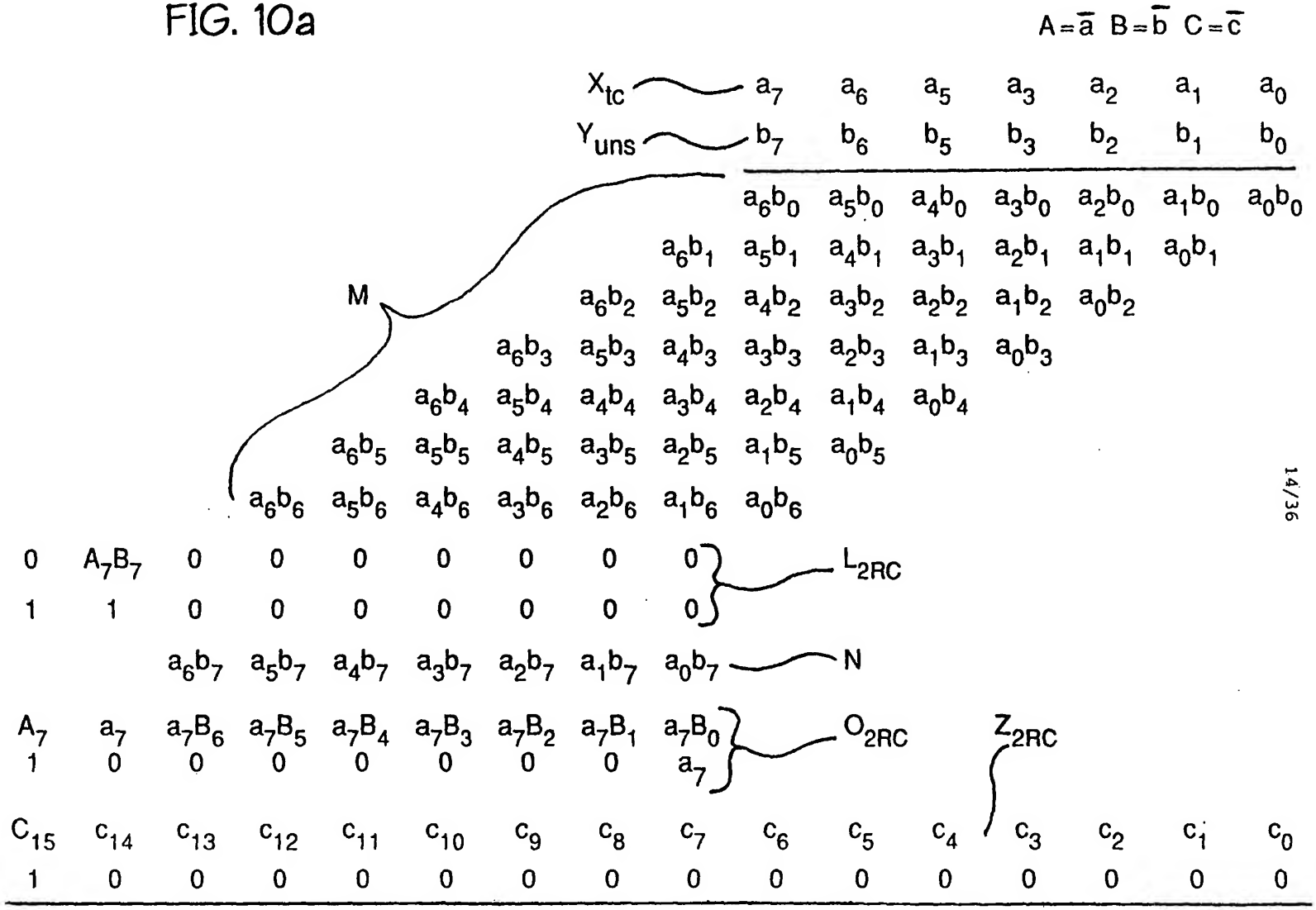

A=$\bar{a}$ B=$\bar{b}$ C=$\bar{c}$
X_{tc}
Y_{uns}
a_7 a_6 a_5 a_3 a_2 a_1 a_0
b_7 b_6 b_5 b_3 b_2 b_1 b_0
M
a_6b_0 a_5b_0 a_4b_0 a_3b_0 a_2b_0 a_1b_0 a_0b_0
a_6b_1 a_5b_1 a_4b_1 a_3b_1 a_2b_1 a_1b_1 a_0b_1
a_6b_2 a_5b_2 a_4b_2 a_3b_2 a_2b_2 a_1b_2 a_0b_2
a_6b_3 a_5b_3 a_4b_3 a_3b_3 a_2b_3 a_1b_3 a_0b_3
a_6b_4 a_5b_4 a_4b_4 a_3b_4 a_2b_4 a_1b_4 a_0b_4
a_6b_5 a_5b_5 a_4b_5 a_3b_5 a_2b_5 a_1b_5 a_0b_5
a_6b_6 a_5b_6 a_4b_6 a_3b_6 a_2b_6 a_1b_6 a_0b_6
0 A_7B_7 0 0 0 0 0 0 0
1 1 0 0 0 0 0 0 0
L_{2RC}
a_6b_7 a_5b_7 a_4b_7 a_3b_7 a_2b_7 a_1b_7 a_0b_7
N
A_7 a_7 a_7B_6 a_7B_5 a_7B_4 a_7B_3 a_7B_2 a_7B_1 a_7B_0
1 0 0 0 0 0 0 0 a_7
O_{2RC}
Z_{2RC}
C_{15} c_{14} c_{13} c_{12} c_{11} c_{10} c_9 c_8 c_7 c_6 c_5 c_4 c_3 c_2 c_1 c_0
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

FIG. 10b

$A=\overline{a}\ B=b\ \overline{C=c}$

								a_7	a_6	a_5	a_3	a_2	a_1	a_0	
								b_7	b_6	b_5	b_3	b_2	b_1	b_0	
								a_6b_0	a_5b_0	a_4b_0	a_3b_0	a_2b_0	a_1b_0	a_0b_0	
							a_7B_0	a_6b_1	a_5b_1	a_4b_1	a_3b_1	a_2b_1	a_1b_1	a_0b_1	
						a_7B_1	a_6b_2	a_5b_2	a_4b_2	a_3b_2	a_2b_2	a_1b_2	a_0b_2		
					a_7B_2	a_6b_3	a_5b_3	a_4b_3	a_3b_3	a_2b_3	a_1b_3	a_0b_3			
				a_7B_3	a_6b_4	a_5b_4	a_4b_4	a_3b_4	a_2b_4	a_1b_4	a_0b_4				
			a_7B_4	a_6b_5	a_5b_5	a_4b_5	a_3b_5	a_2b_5	a_1b_5	a_0b_5					
		a_7B_5	a_6b_6	a_5b_6	a_4b_6	a_3b_6	a_2b_6	a_1b_6	a_0b_6						
1	A_7B_7	a_7B_6	a_6b_6	a_5b_6	a_4b_6	a_3b_6	a_2b_6	a_1b_6	a_0b_6						
		a_6b_7	a_5b_7	a_4b_7	a_3b_7	a_2b_7	a_1b_7	a_0b_7							
A_7	a_7						a_7								
C_{15}	c_{14}	c_{13}	c_{12}	c_{11}	c_{10}	c_9	c_8	c_7	c_6	c_5	c_4	c_3	c_2	c_1	c_0

FIG. 10c

$A=\overline{a}$ $B=\overline{b}$ $C=\overline{c}$

c_7 a_7B_0 a_6b_1	c_6 a_6b_0 a_5b_1	c_5 a_5b_0 a_4b_1	c_4 a_4b_0 a_3b_1	c_3 a_3b_0 a_2b_1	c_2 a_2b_0 a_1b_1	c_1 a_1b_0 a_0b_1	c_0 a_0b_0
c_8 a_7B_1 a_6b_2	a_5b_2 a_7	a_4b_2	a_3b_2	a_2b_2	a_1b_2	a_0b_2	
c_9 a_7B_2 a_6b_3	a_5b_3	a_4b_3	a_3b_3	a_2b_3	a_1b_3	a_0b_3	
c_{10} a_7B_3 a_6b_4	a_5b_4	a_4b_4	a_3b_4	a_2b_4	a_1b_4	a_0b_4	
c_{11} a_7B_4 a_6b_5	a_5b_5	a_4b_5	a_3b_5	a_2b_5	a_1b_5	a_0b_5	
c_{12} a_7B_5 a_6b_6	a_5b_6	a_4b_6	a_3b_6	a_2b_6	a_1b_6	a_0b_6	
c_{13} a_7B_6 a_6b_7	a_5b_7	a_4b_7	a_3b_7	a_2b_7	a_1b_7	a_0b_7	

C_{15}	A_7B_7
A_7	a_7
1	c_{14}
	1

FIG. 11a

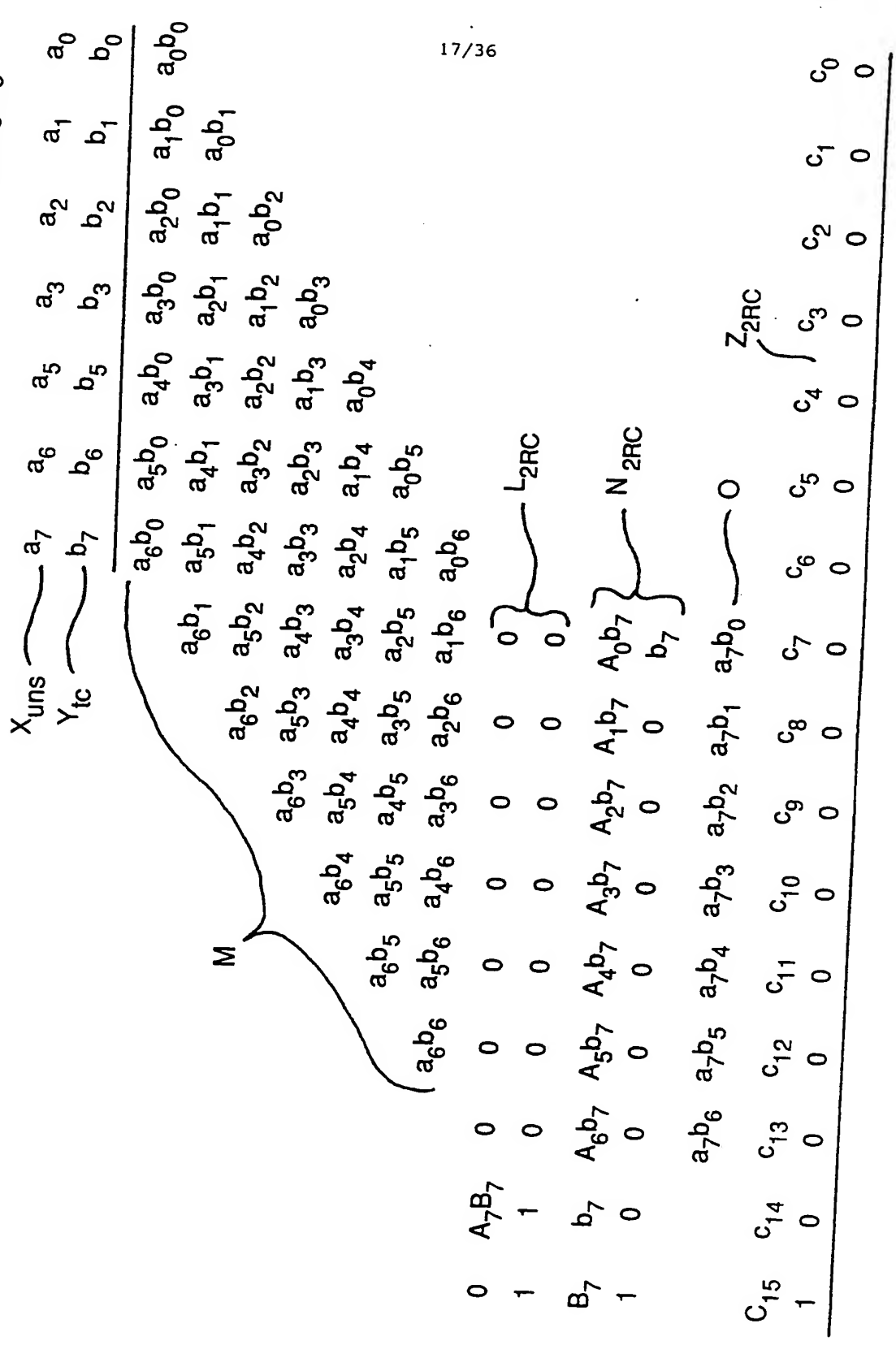


FIG. 11b

$A = \bar{a}$ $B = \bar{b}$ $C = \bar{c}$

									a_7	a_6	a_5	a_3	a_2	a_1	a_0
									b_7	b_6	b_5	b_3	b_2	b_1	b_0
								a_7b_0	a_6b_0	a_5b_0	a_4b_0	a_3b_0	a_2b_0	a_1b_0	a_0b_0
							a_7b_1	a_6b_1	a_5b_1	a_4b_1	a_3b_1	a_2b_1	a_1b_1	a_0b_1	
						a_7b_2	a_6b_2	a_5b_2	a_4b_2	a_3b_2	a_2b_2	a_1b_2	a_0b_2		
					a_7b_3	a_6b_3	a_5b_3	a_4b_3	a_3b_3	a_2b_3	a_1b_3	a_0b_3			
				a_7b_4	a_6b_4	a_5b_4	a_4b_4	a_3b_4	a_2b_4	a_1b_4	a_0b_4				
	1		a_7b_5	a_6b_5	a_5b_5	a_4b_5	a_3b_5	a_2b_5	a_1b_5	a_0b_5					
1	A_7B_7	a_7b_6	a_6b_6	a_5b_6	a_4b_6	a_3b_6	a_2b_6	a_1b_6	a_0b_6						
B_7	b_7	A_6b_7	A_5b_7	A_4b_7	A_3b_7	A_2b_7	A_1b_7	A_0b_7							
								b_7							
C_{15}	c_{14}	c_{13}	c_{12}	c_{11}	c_{10}	c_9	c_8	c_7	c_6	c_5	c_4	c_3	c_2	c_1	c_0

FIG. 11c

$A = \overline{a}$ $B = \overline{b}$ $C = \overline{c}$

c_7 a_7b_0 a_6b_1	c_6 a_6b_0 a_5b_1	c_5 a_5b_0 a_4b_1	c_4 a_4b_0 a_3b_1	c_3 a_3b_0 a_2b_1	c_2 a_2b_0 a_1b_1	c_1 a_1b_0 a_0b_1	c_0 a_0b_0
c_8 a_7b_1 a_6b_2	a_5b_2	a_4b_2	a_3b_2	a_2b_2	a_1b_2	a_0b_2	
c_9 a_7b_2 a_6b_3	a_5b_3	a_4b_3	a_3b_3	a_2b_3	a_1b_3	a_0b_3	
c_{10} a_7b_3 a_6b_4	a_5b_4	a_4b_4	a_3b_4	a_2b_4	a_1b_4	a_0b_4	
c_{11} a_7b_4 a_6b_5	a_5b_5	a_4b_5	a_3b_5	a_2b_5	a_1b_5	a_0b_5	
c_{12} a_7b_5 a_6b_6	a_5b_6	a_4b_6	a_3b_6	a_2b_6	a_1b_6	a_0b_6	
c_{13} a_7b_6 A_6b_7	A_5b_7	A_4b_7	A_3b_7	A_2b_7	A_1b_7	A_0b_7 b_7	

C_{15} B_7	A_7B_7 b_7
1	c_{14} 1

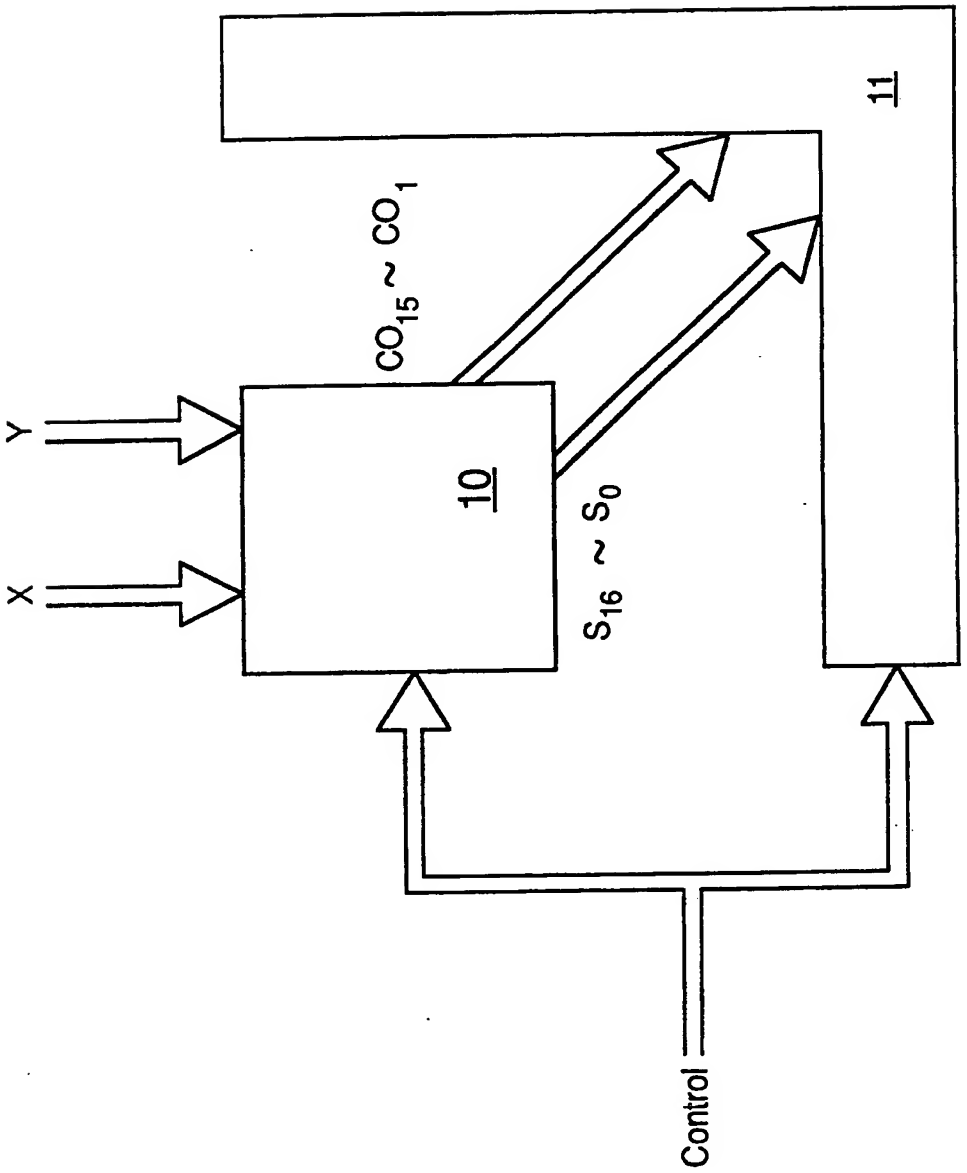


FIG. 12a

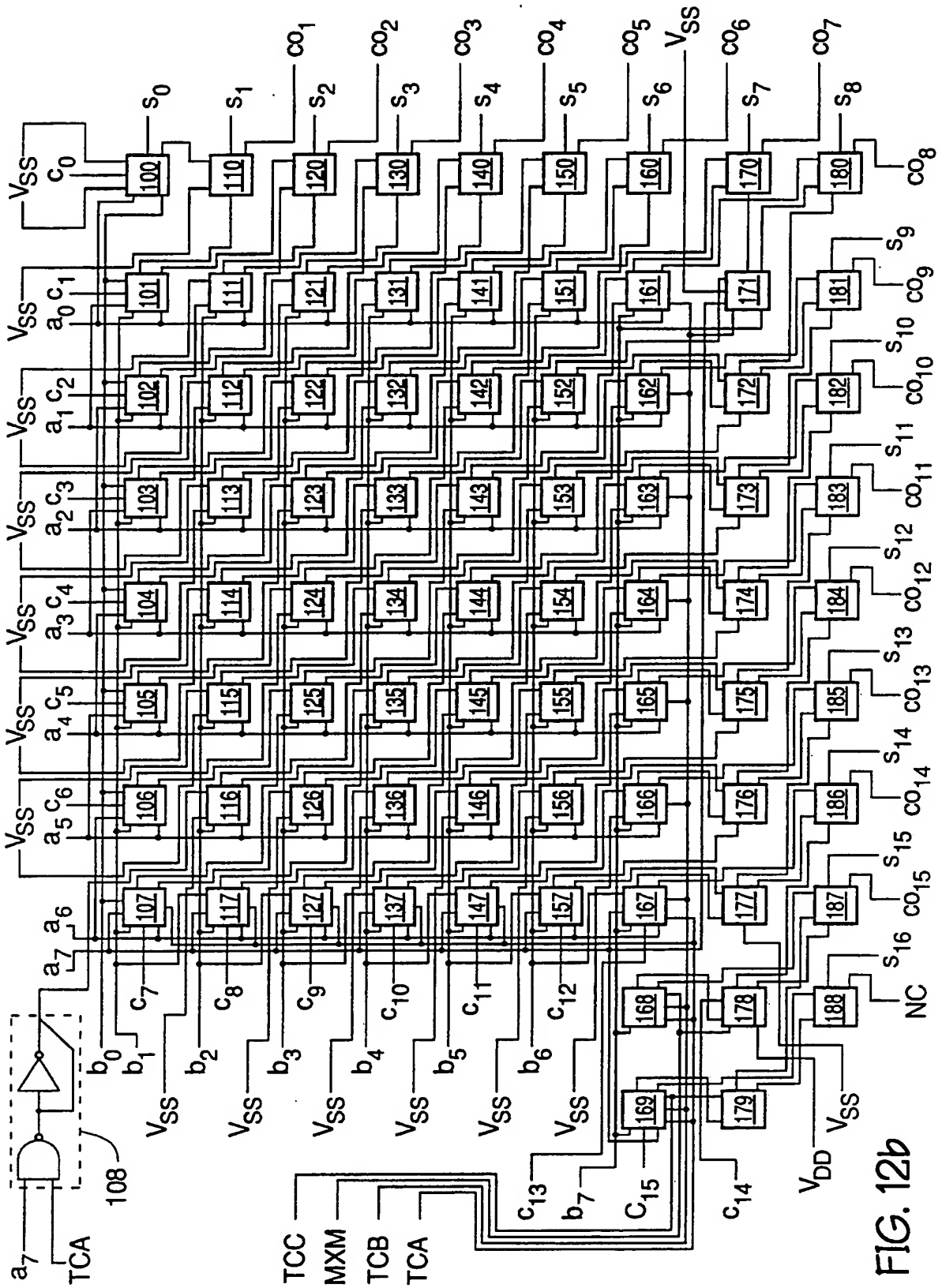

V_{SS} c_0 100 s_0 co_1
V_{SS} a_0 c_1 101 110 s_1 co_2
V_{SS} a_1 c_2 102 111 120 s_2 co_3
V_{SS} a_2 c_3 103 112 121 130 s_3 co_4
V_{SS} a_3 c_4 104 113 122 131 140 s_4 co_5
V_{SS} a_4 c_5 105 114 123 132 141 150 s_5 co_6
V_{SS} a_5 c_6 106 115 124 133 142 151 160 s_6 V_{SS}
a_6 107 116 125 134 143 152 161 170 s_7 co_7
a_7 117 126 135 144 153 162 171 180 s_8 co_8
127 136 145 154 163 172 181 s_9 co_9
137 146 155 164 173 182 s_{10} co_{10}
147 156 165 174 183 s_{11} co_{11}
157 166 175 184 s_{12} co_{12}
167 176 185 s_{13} co_{13}
177 186 s_{14} co_{14}
187 s_{15} co_{15}
s_{16} NC
b_0 b_1 b_2 b_3 b_4 b_5 b_6 b_7
c_7 c_8 c_9 c_{10} c_{11} c_{12} c_{13} c_{14} c_{15}
168 178 188
169 179
V_{SS} V_{SS} V_{SS} V_{SS} V_{SS} V_{SS} V_{SS} V_{DD} V_{SS}
108
a_7 TCA TCC MXM TCB TCA

FIG. 12b

FIG. 13a

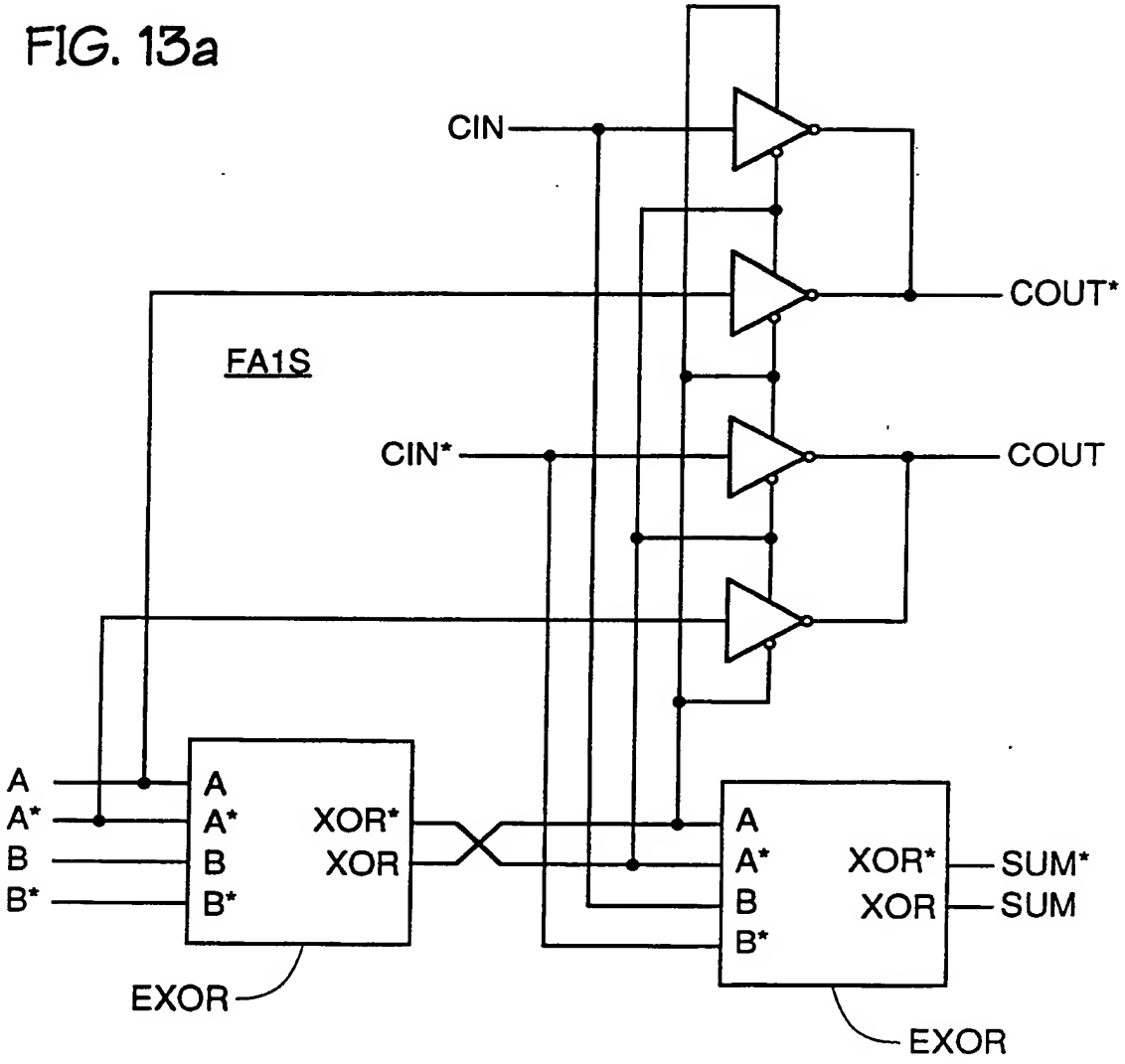


FIG. 13b

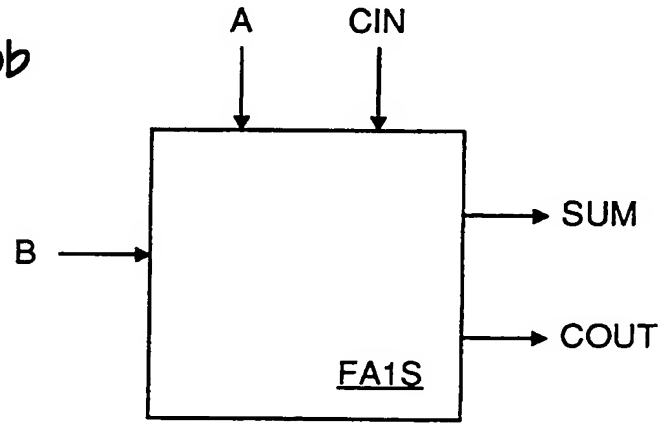


FIG. 14a

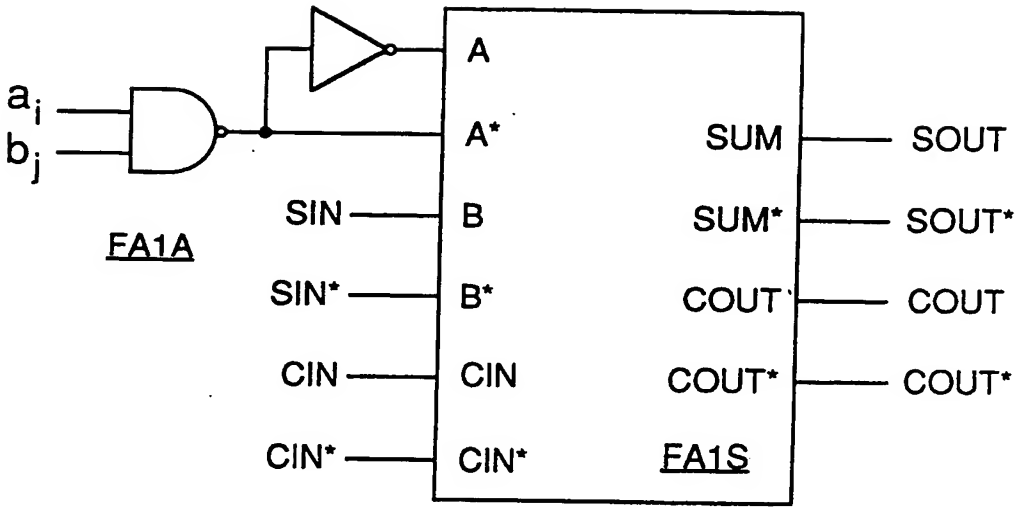


FIG. 14b

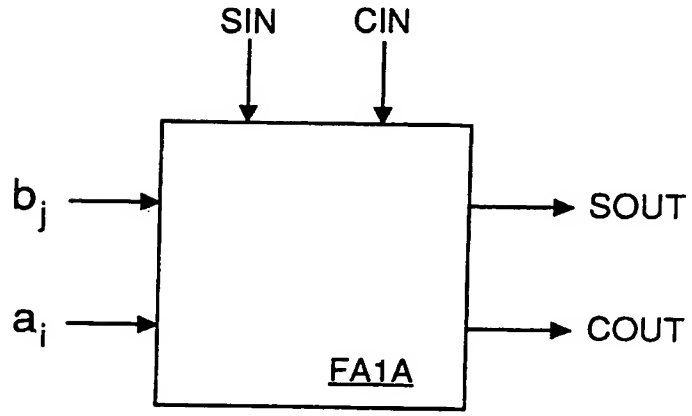


FIG. 15a

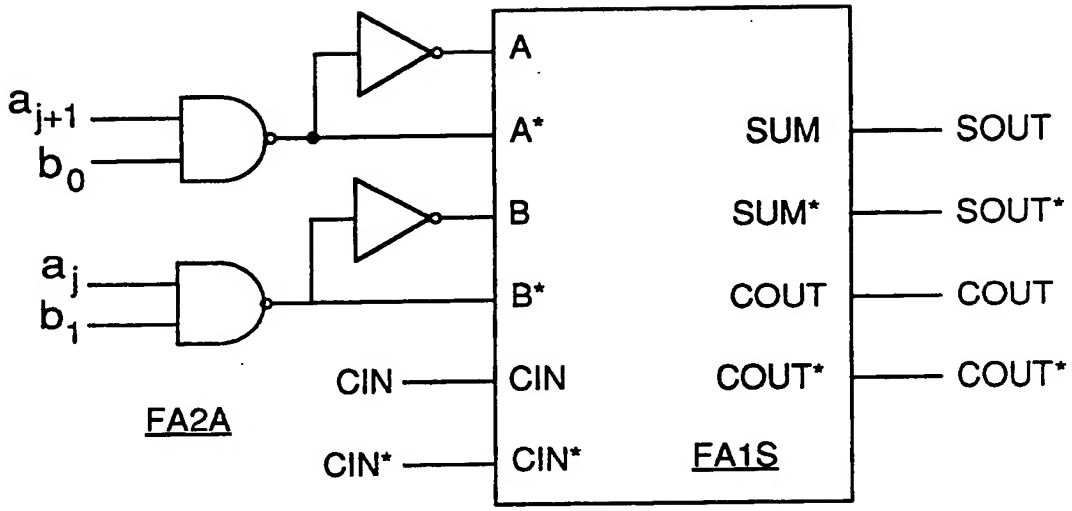
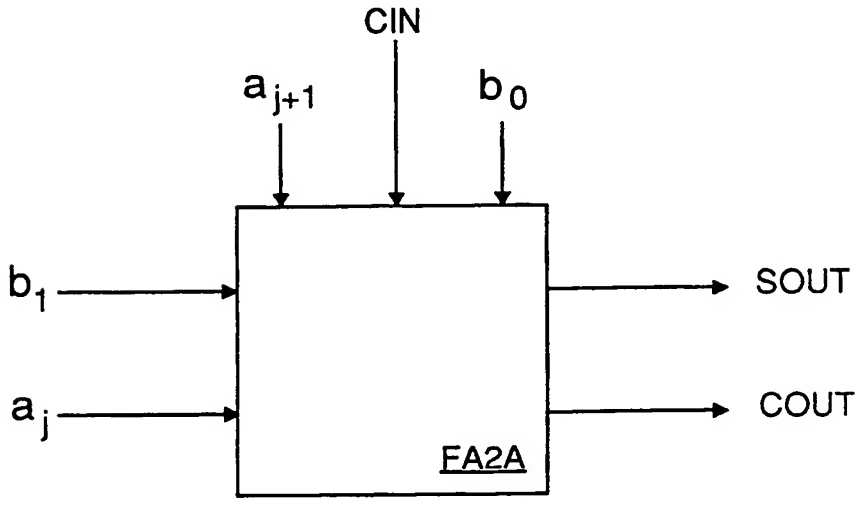


FIG. 15b



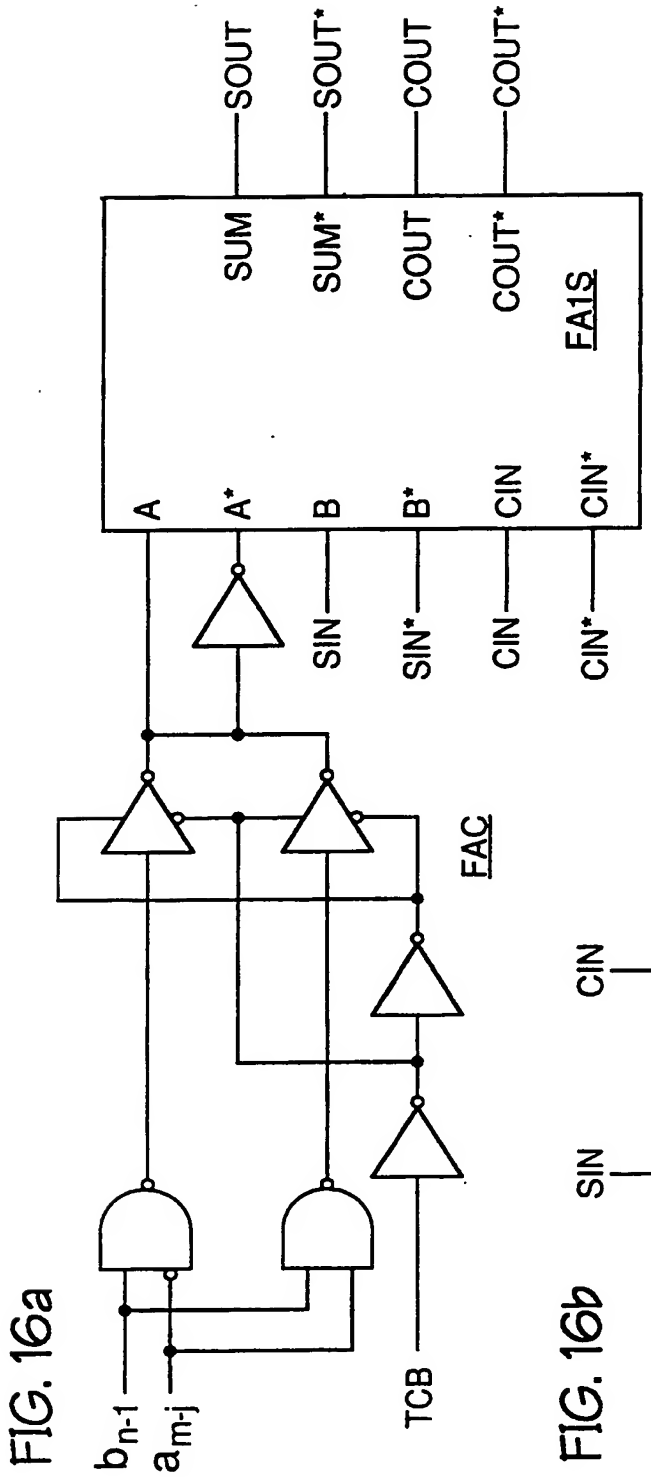


FIG. 16a

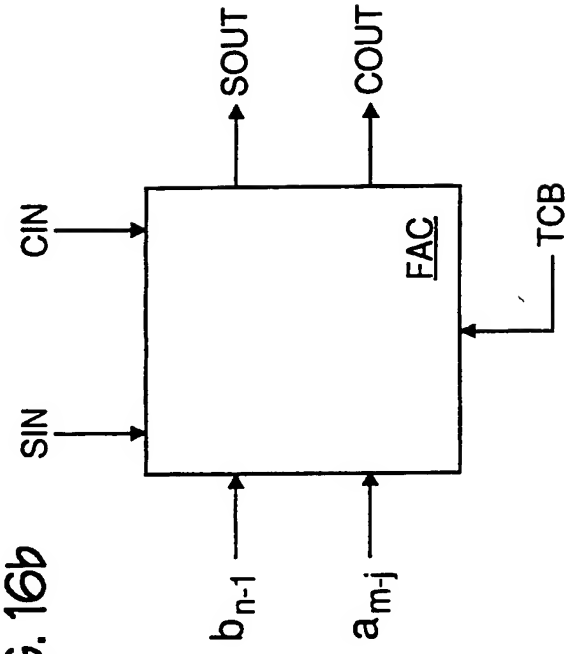


FIG. 16b

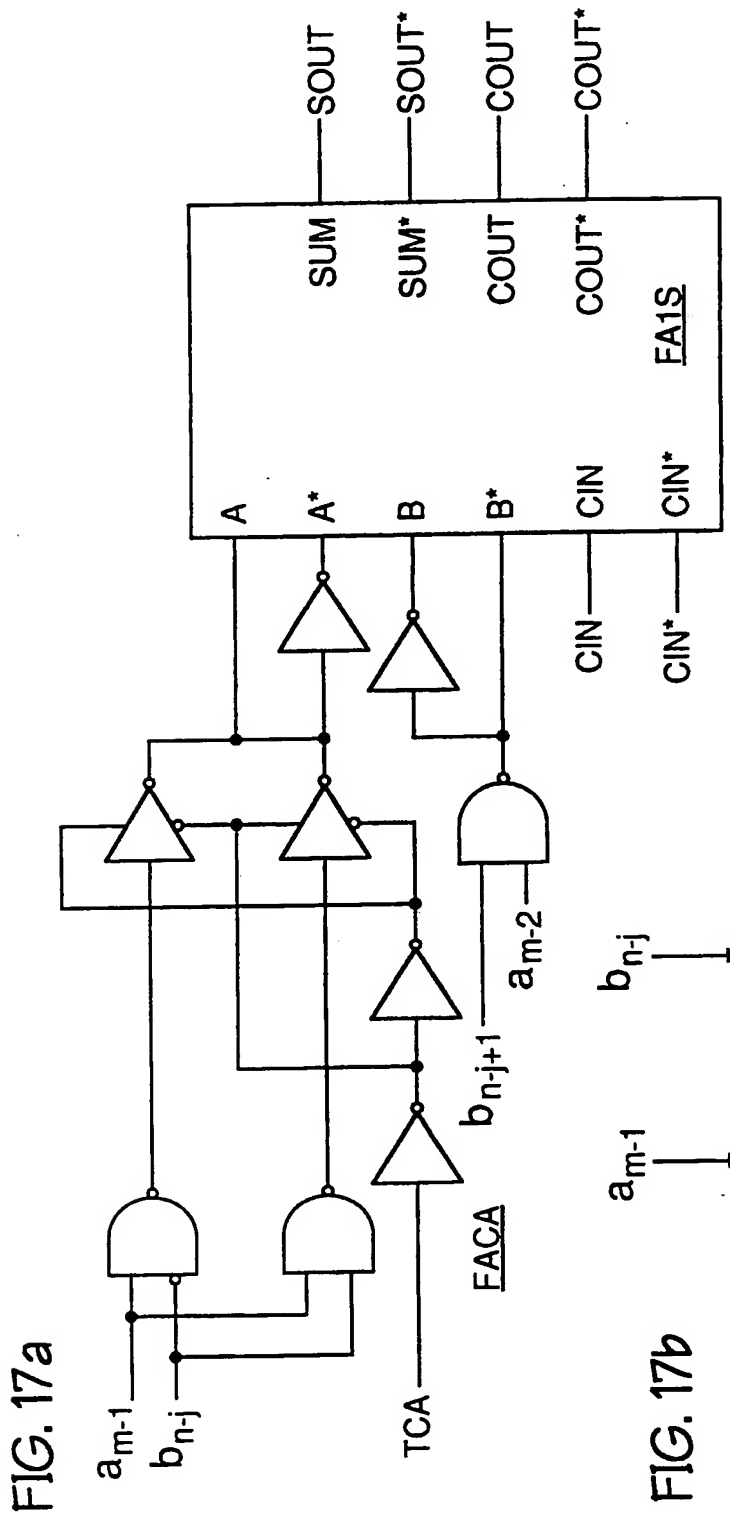


FIG. 17a

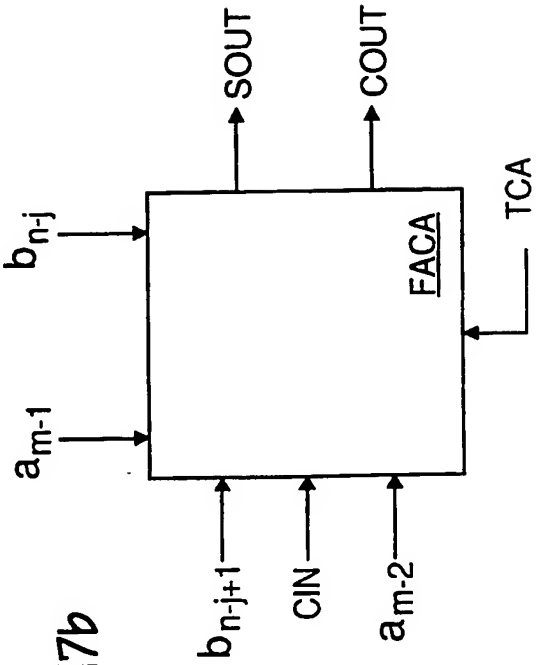


FIG. 17b

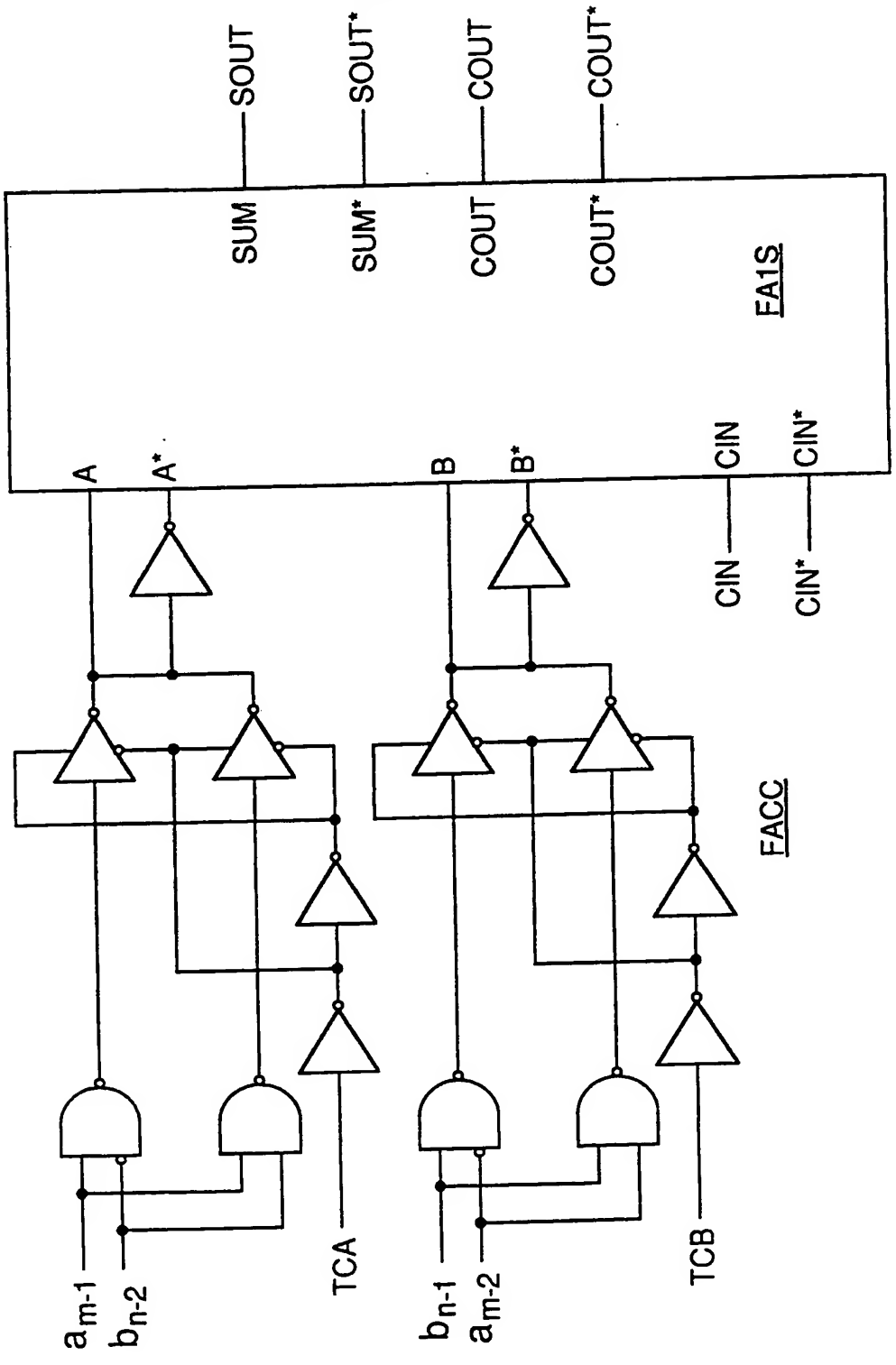

SOUT
SOUT*
COUT
COUT*
SUM
SUM*
COUT
COUT*
FA1S
A
A*
B
B*
CIN
CIN*
CIN
CIN*
FACC
TCA
TCB
a_{m-1}
b_{n-2}
b_{n-1}
a_{m-2}

FIG. 18a

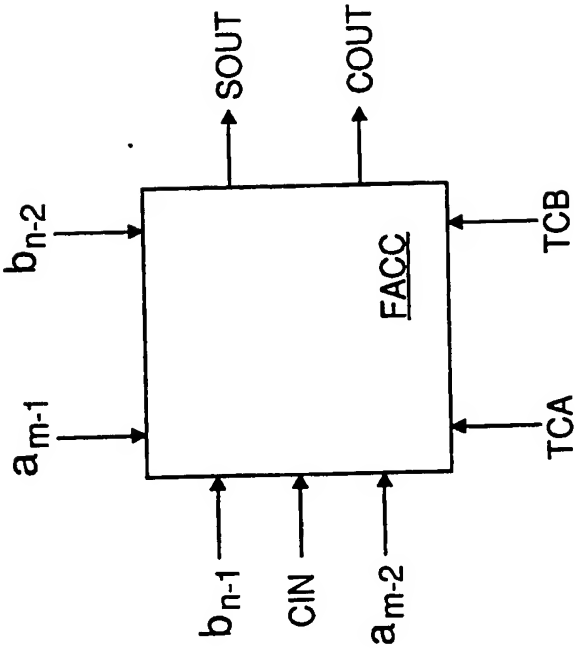


FIG. 18b

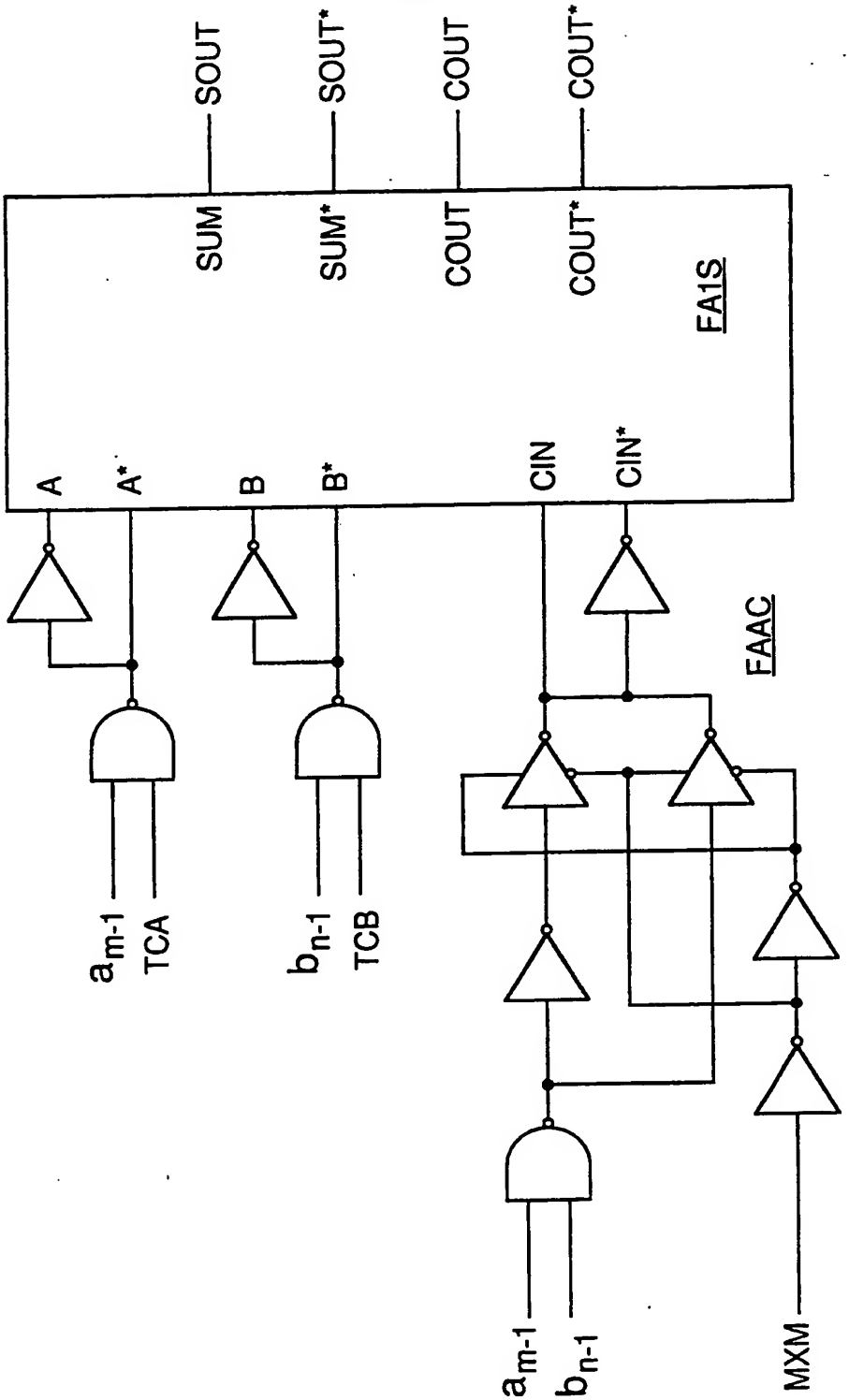

SOUT
SOUT*
COUT
COUT*
SUM
SUM*
COUT
COUT*
FA1S
A
A*
B
B*
CIN
CIN*
FAAC
a_{m-1}
TCA
b_{n-1}
TCB
a_{m-1}
b_{n-1}
MXM

FIG. 19a

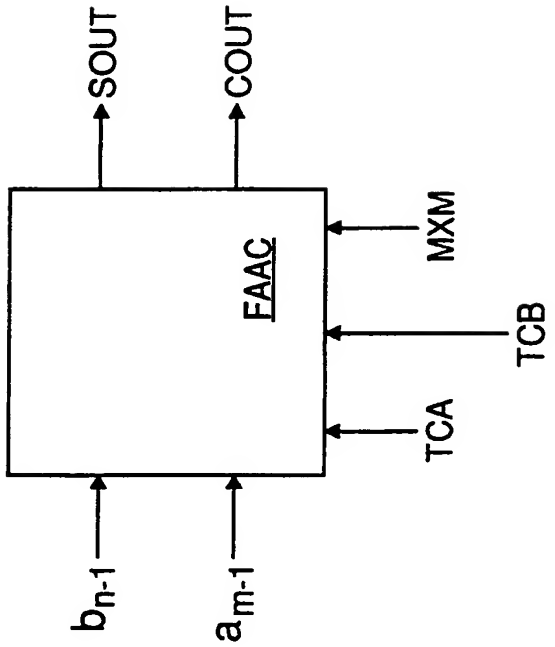


FIG. 19b

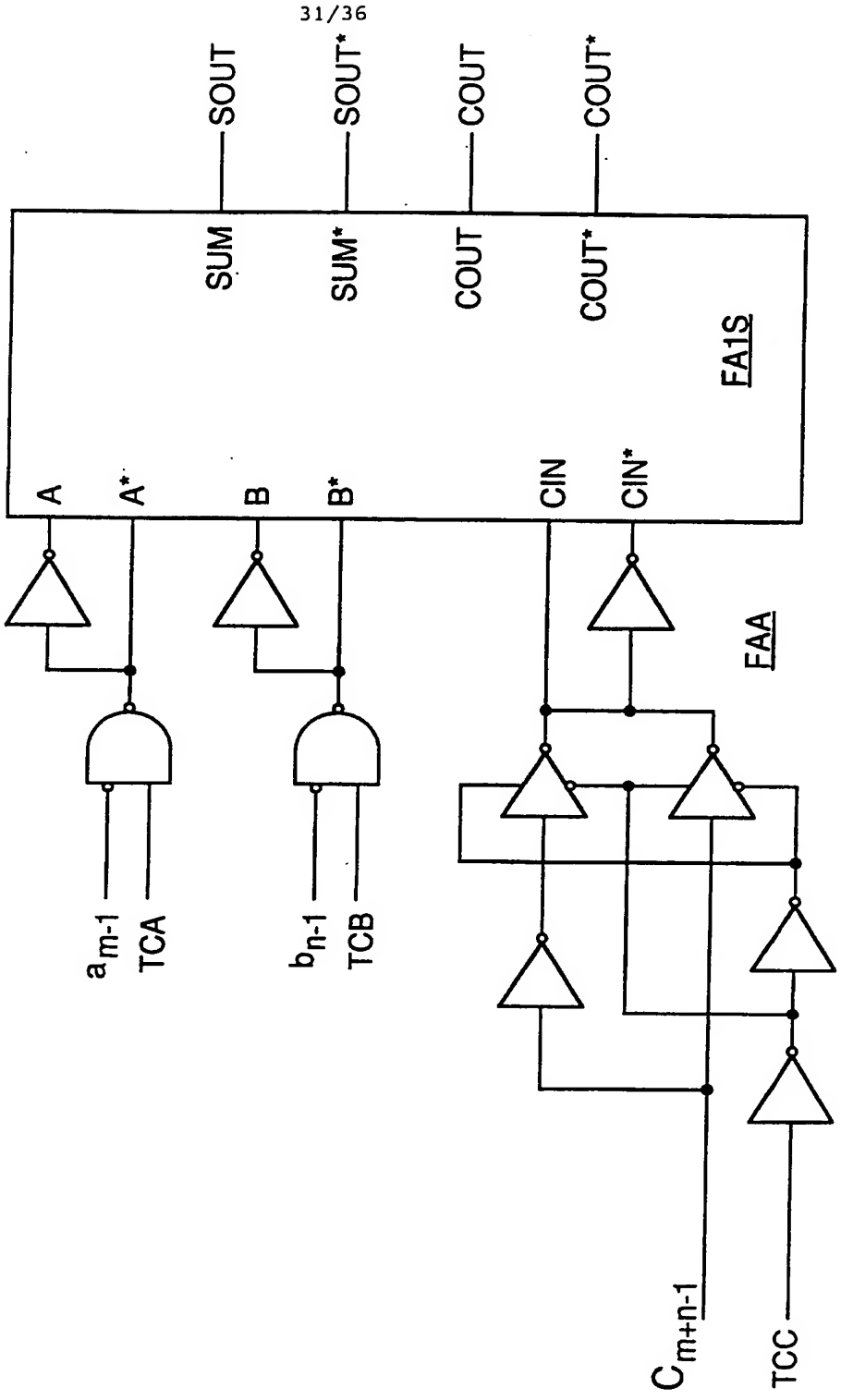

SOUT
SOUT*
COUT
COUT*
SUM
SUM*
COUT
COUT*
FA1S
A
A*
B
B*
CIN
CIN*
FAA
a_{m-1}
TCA
b_{n-1}
TCB
C_{m+n-1}
TCC

FIG. 20a

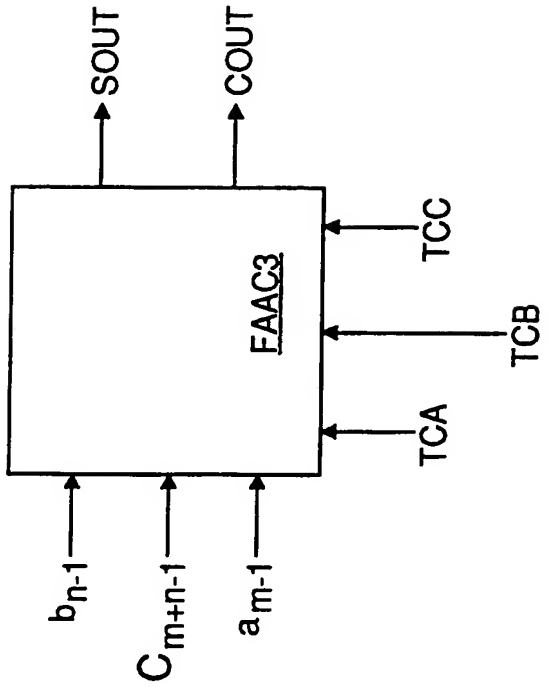


FIG. 20b

FIG. 21a

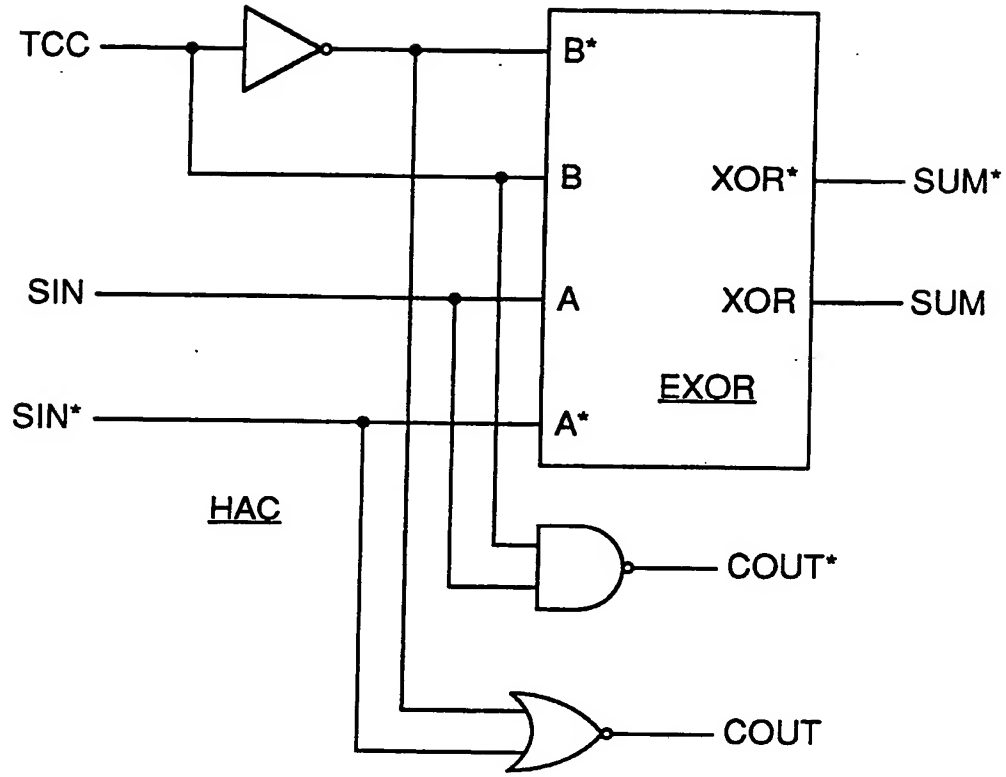


FIG. 21b

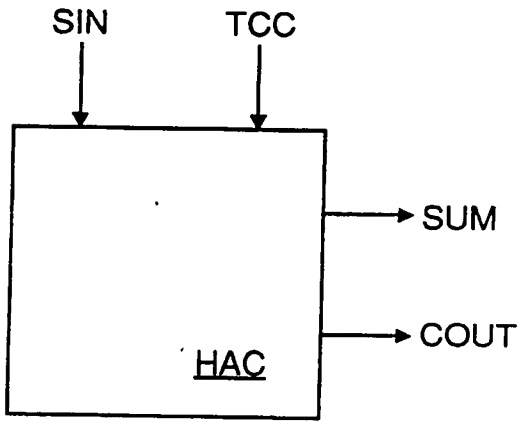


FIG. 22a

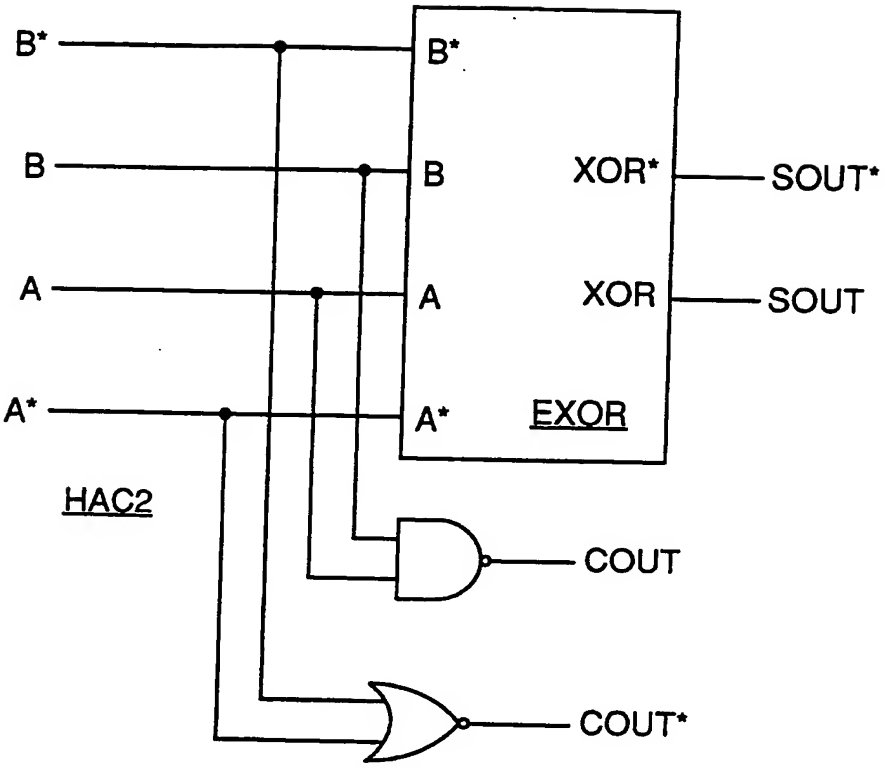


FIG. 22b

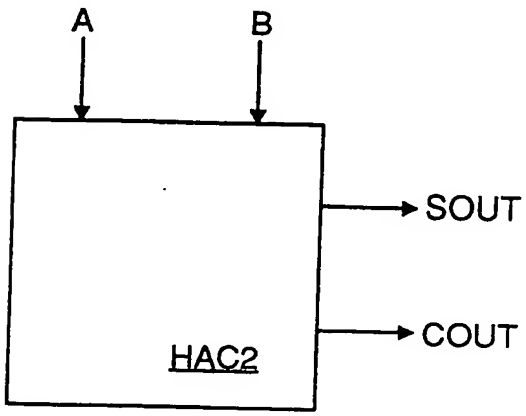
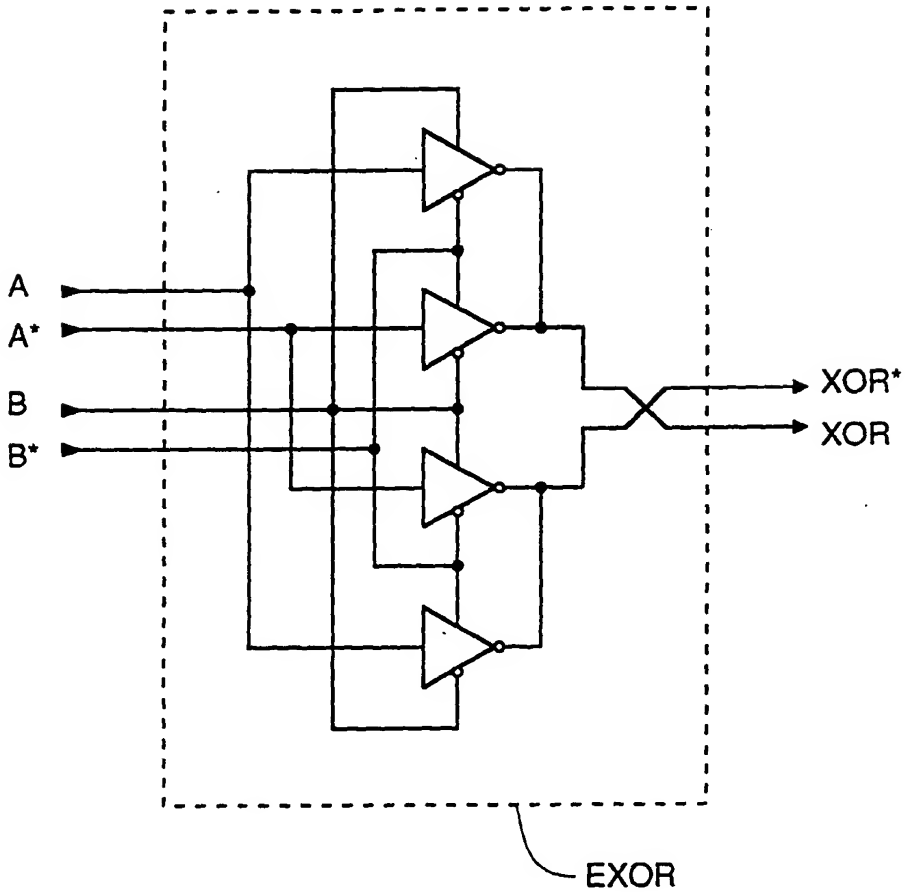


FIG. 23



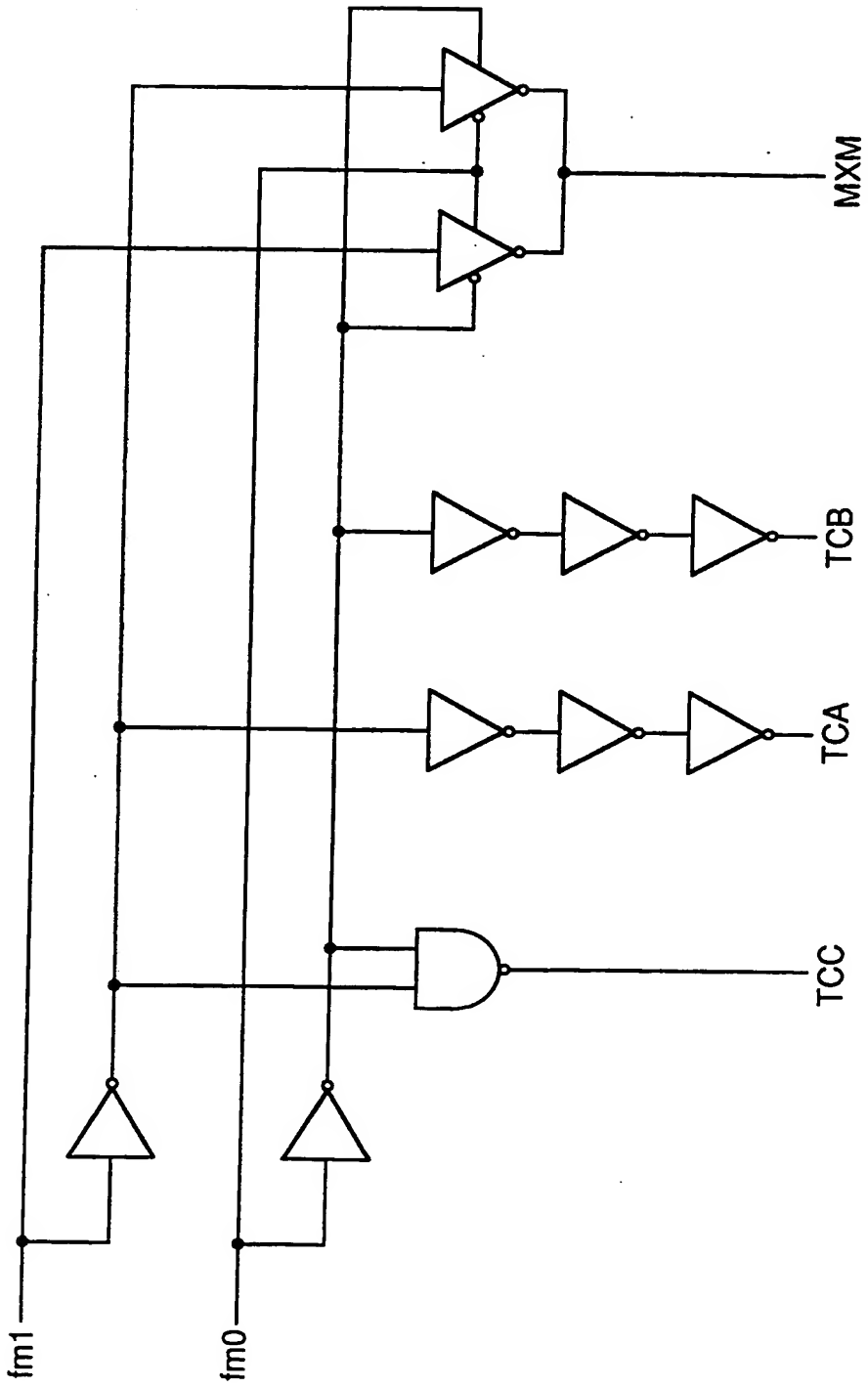


FIG. 24

INTERNATIONAL SEARCH REPORT

International Application No PCT/US91/00823

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC(5): G06F 7/52
US CL.: 364/757,758

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
US	364/757,758,759

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category [6]	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
A	US, A, 4,706,210 (SNELLING et al.) 10 November 1987 See entire document.	1-29
A	US, A, 4,831,577 (WEI et al.) 16 May 1989 See entire document.	1-29
A	US, A, 4,839,848 (PETERSON et al.) 13 June 1989 See entire document.	1-29
A	US, A, 3,866,030 (BAUGH et al.) 11 February 1975 See entire document.	1-29

[6] Special categories of cited documents: [15]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search [3]	Date of Mailing of this International Search Report [3]
10 APRIL 1991	22 MAY 1991
International Searching Authority [1]	Signature of Authorized Officer [20]
ISA/US	D.H. MALZAHN